

LYON-External

CPU :Intel PENRYN
Chip Set :Intel CANTIGA PM + ICH9M
Remarks :Montevina Platform (NB9M)

Model Name : LYON-Ext
PBA Name : MAIN
PCB Code : TPT : BA41-00919A
GCE : BA41-00920A
NAN : BA41-00921A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2008.06.09

DRAW	CHECK	APPROVAL

Owner : SEC Mobile R & D Signature : X

DRAW	TERM1	DATE	1/10/2008	TITLE	L YON-External COVER	SAMSUNG ELECTRONICS PART NO. BA41-00920A
CHECK	HJ KIM	DEV. STEP	MP			
APPROVAL	SJ PARK	REV	1.0			
ROUTE CODE	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	1 OF 19		

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices			
Devices	IDSEL #	REQ/GNT#	Interrupts
Cardbus	AD25	3	A, B, C
USB	AD29 (internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHC0) : H
Hub to PCI LPC bridge/IDE/AC97/SMBUS	AD30 (internal) AD31 (internal)	- -	- B
Internal MAC	AD24 (internal)	-	E
AC Link	-	-	F
GLAN	-	-	F

	Voltage Rails
VDC, CORE	Primary DC system power supply (7 to 21V)
VFX, CORE	Core Voltage for CPU
P1.6V (VCCP)	1.6V Core Voltage for CPU
P1.5V (VCCM)	1.5V Core Voltage for CPU
P1.8V	1.8V Core Voltage for CPU
P1.8V_AUX	1.8V switched power rail (off in S3-S5)
P3.3V	3.3V power rail for DDR (off in S3-S5)
P3.3V_AUX	3.3V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched power rail (off in S4-S5)
P5.0V_AUX	5.0V always power rail

USB Port Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
	SYSTEM PORT 0	0	NC
	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
	SYSTEM PORT 2	2	NC
	NC	3	NC
	NC	4	NC
	Bluetooth	5	Mini Card 2 (GROSSON or DVB-T)
	Mini PCI Express 2		
	Camera		
	NC		
	NC		

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IOH8-M	Real Time Clock
Crystal	10MHz	MCOM	HC59F2169/2160
Crystal	14.318MHz	CLOCK Generator	CN-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect (TBD)	
Devices	Resolution
	PANNEL_DETECT_0

Devices	Address	Hex	Bus
IC18-m	Master	-	SMBUS Master
CPU1 Thermal Sensor	0111 101x	7Ah	-
SCD1MM0	0110 010x	7Ah	Thermal Sensor
SCD1MM1	1010 010x	A4h	-
Thermal Sensor on SCD1MM0	0011 000x	30h	-
Thermal Sensor on SCD1MM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

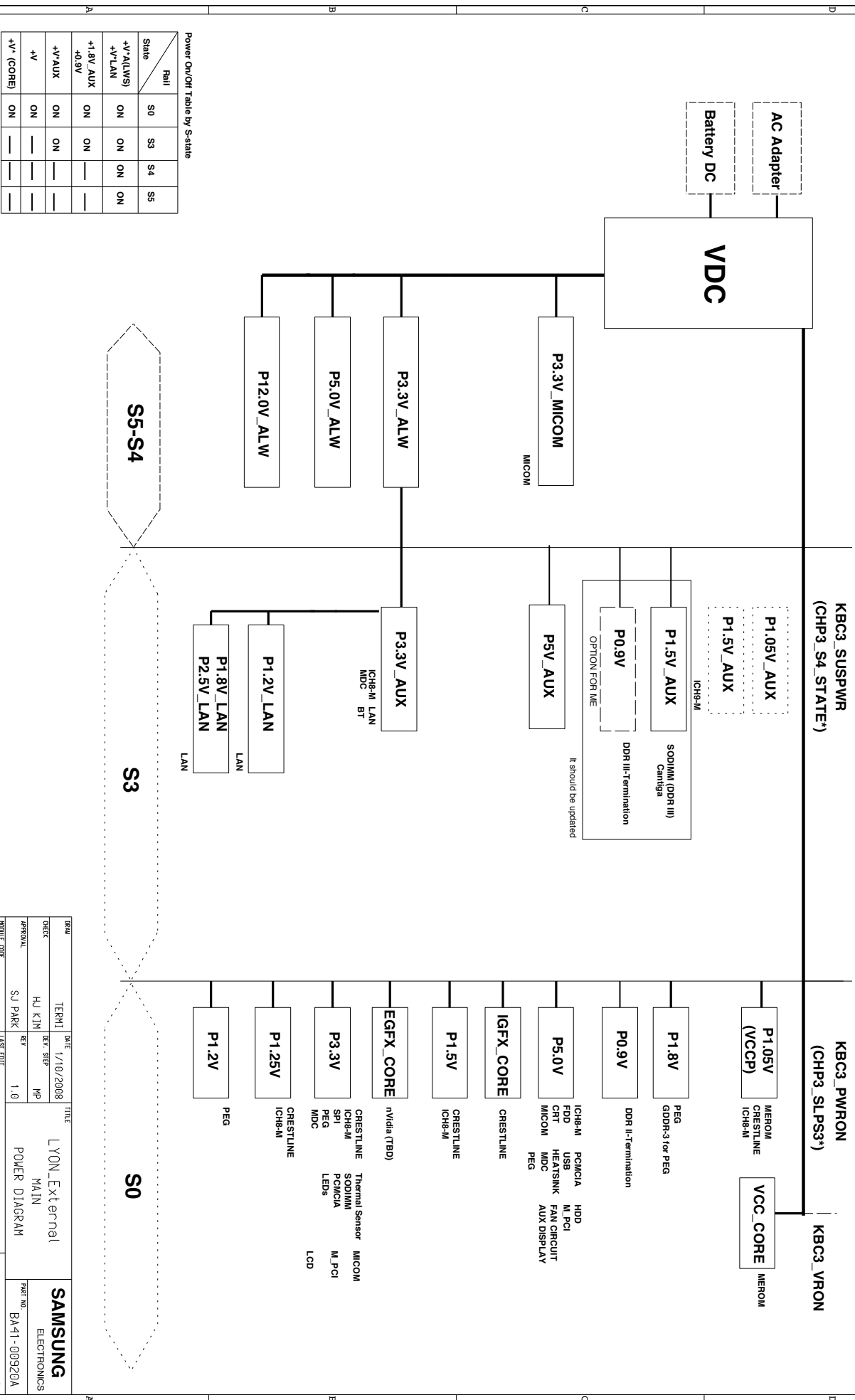
REVISION HISTORY

See rev notes for more information.

DATE	TITLE
TERM1 CHKC HJ KIM APPROVAL S J PARK MOBILE CODE	L YON_External CHIPSET POWER UNDEFINED
DATE REV. STEP HP REV 1.0	
LAST EDIT	PAGE 3 OF 19

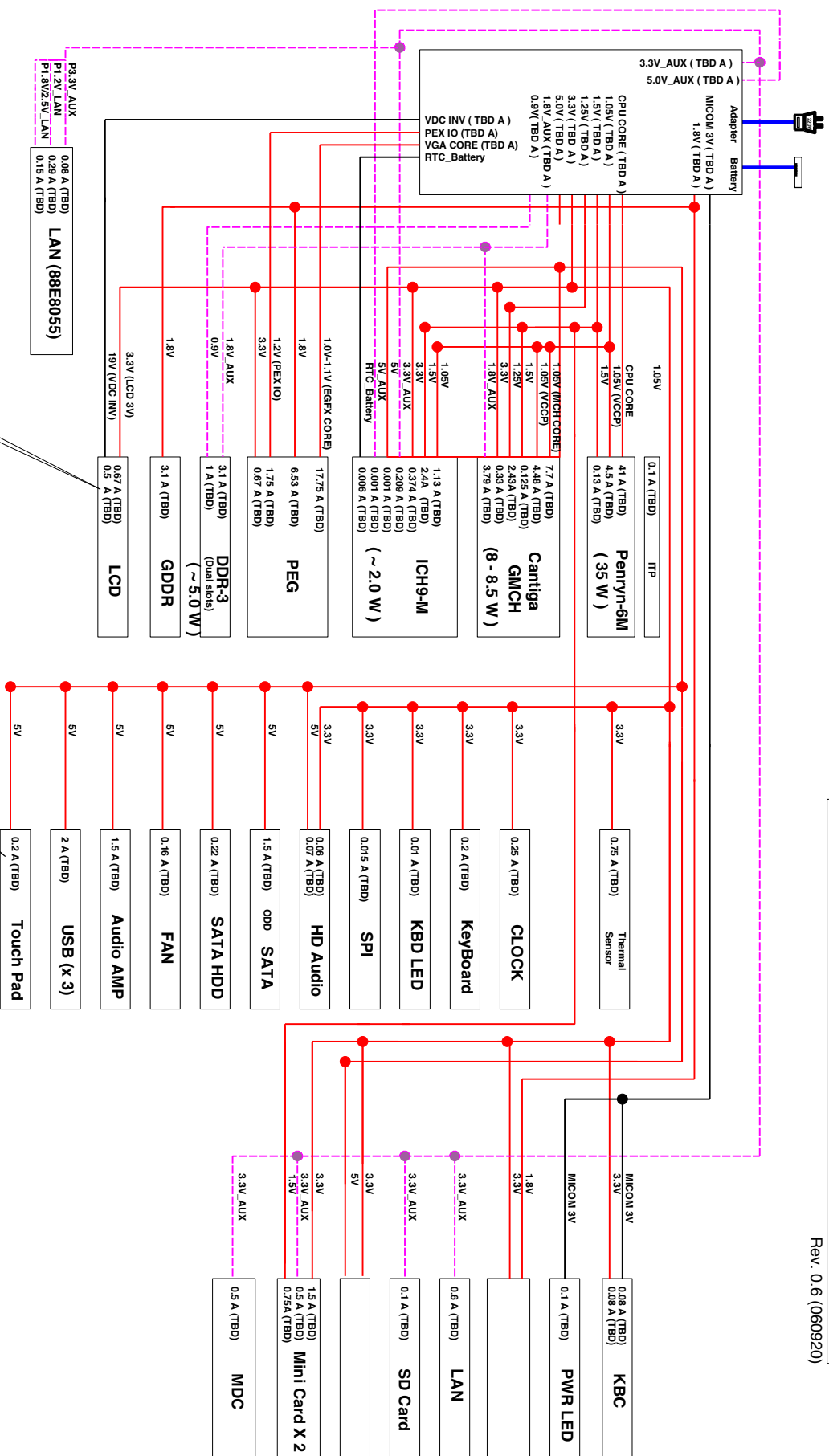
POWER DIAGRAM

Rev 0.1



POWER RAILS ANALYSIS

Rev. 0.6 (060920)

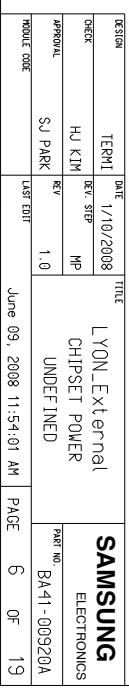


Value by Datasheet/Application notes (Value by measurement)

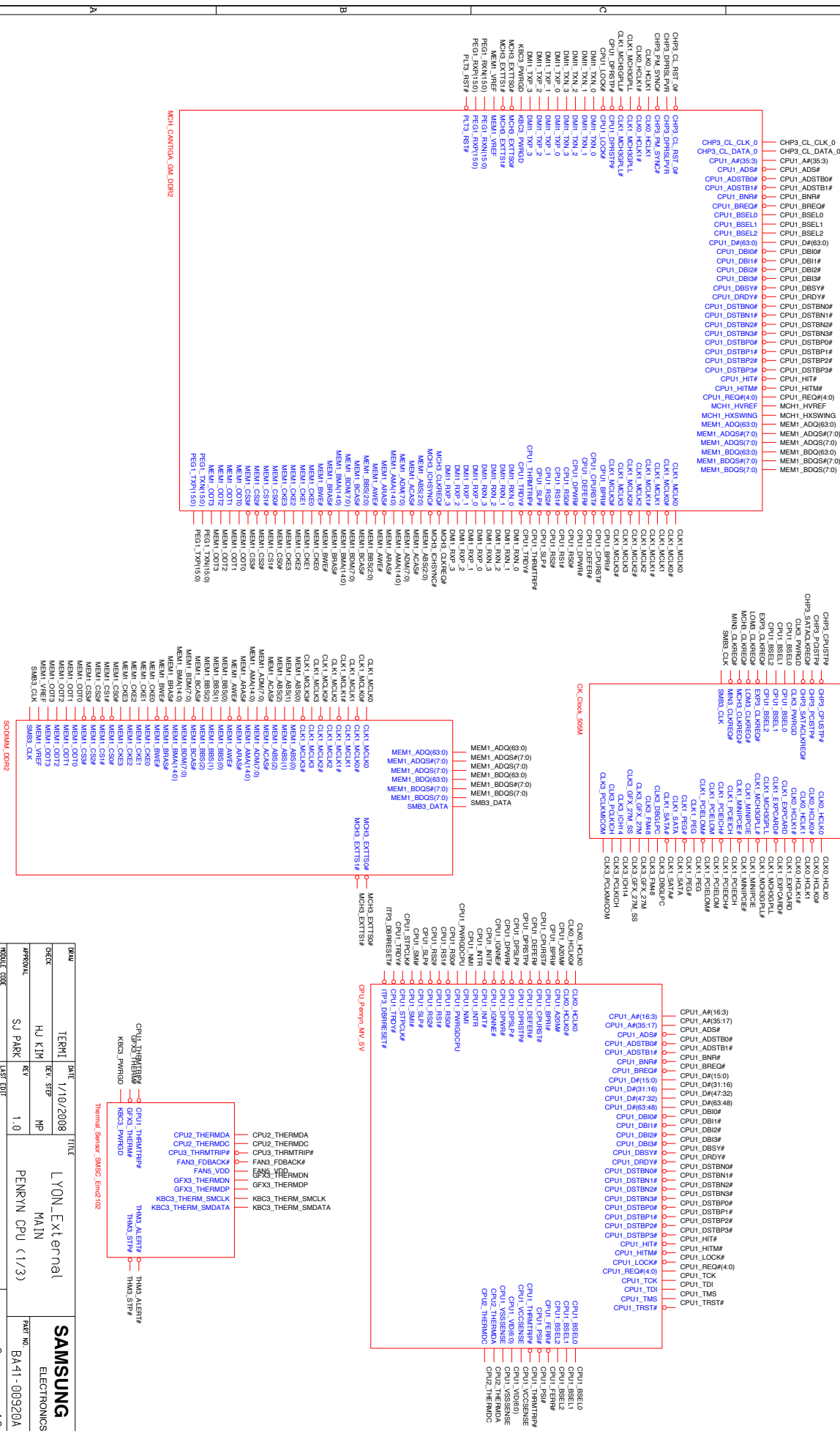
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0001	HJ KIM	1/10/2008	LYON_External
0002	SJ PARK	1/10/2008	CHIPSET POWER
0003	LSH EDIT	1/10/2008	UNDEFINED

DESIGN	DATE	TIME	PAGE
0001	1/10/2008	11:54:01 AM	5 OF 19

REVISION	DATE	TIME	PAGE
0001	1/10/2008	11:54:01 AM	5 OF 19







COM-22C-0156 (1956.6.5) REV. 3

4

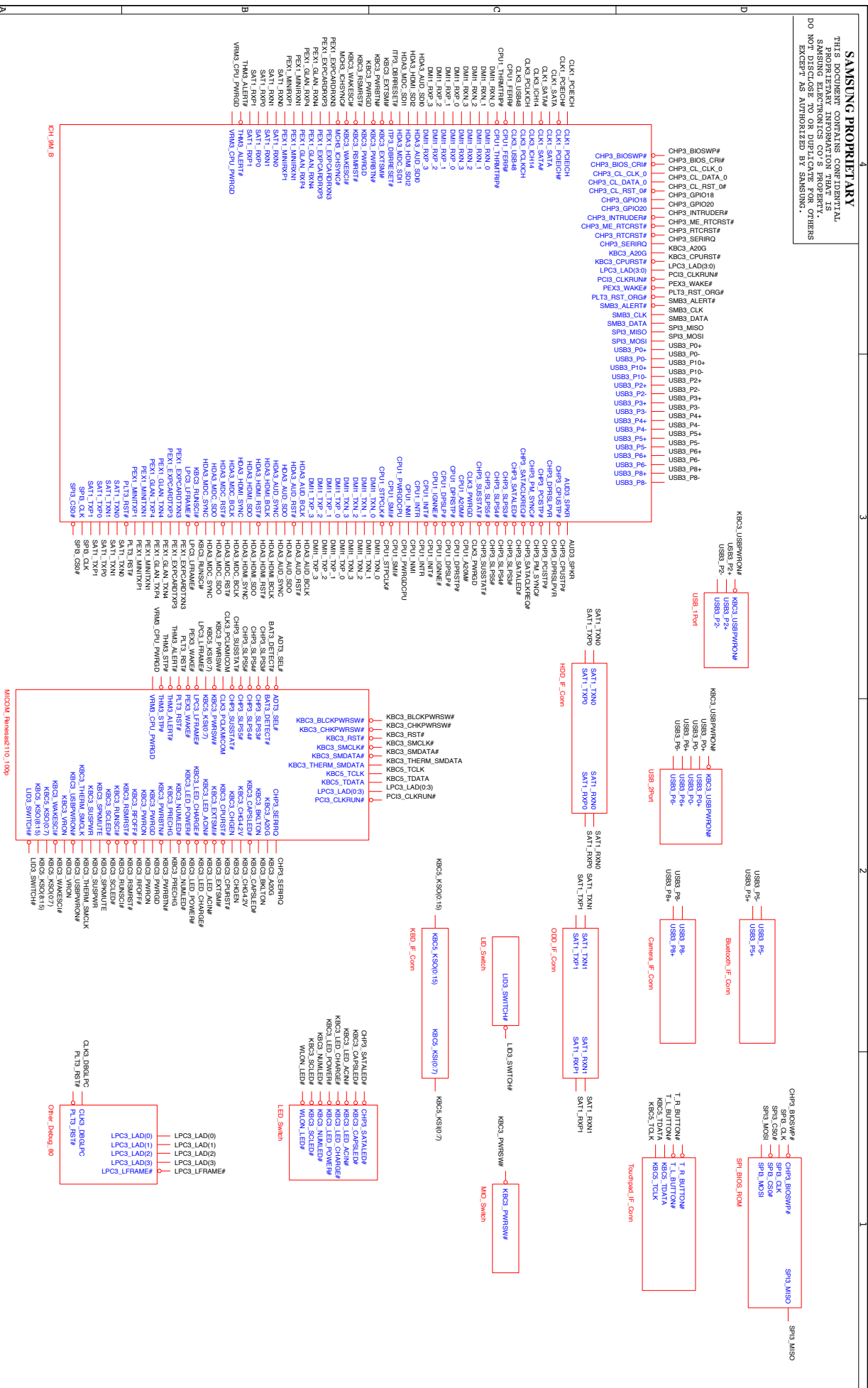
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2

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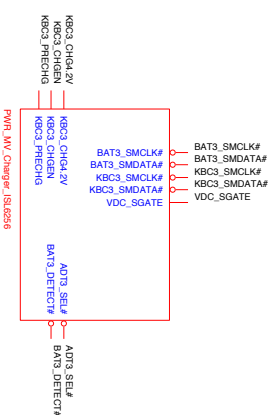
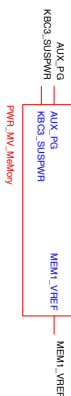
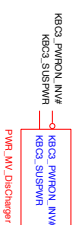
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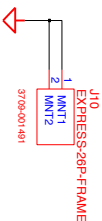


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SU PARK		MP	UNDEFINED
TOTAL CODE		REV: 1.0	
LAST EDIT		June 09, 2008 11:54:01 AM	
PAGE		9	OF 19



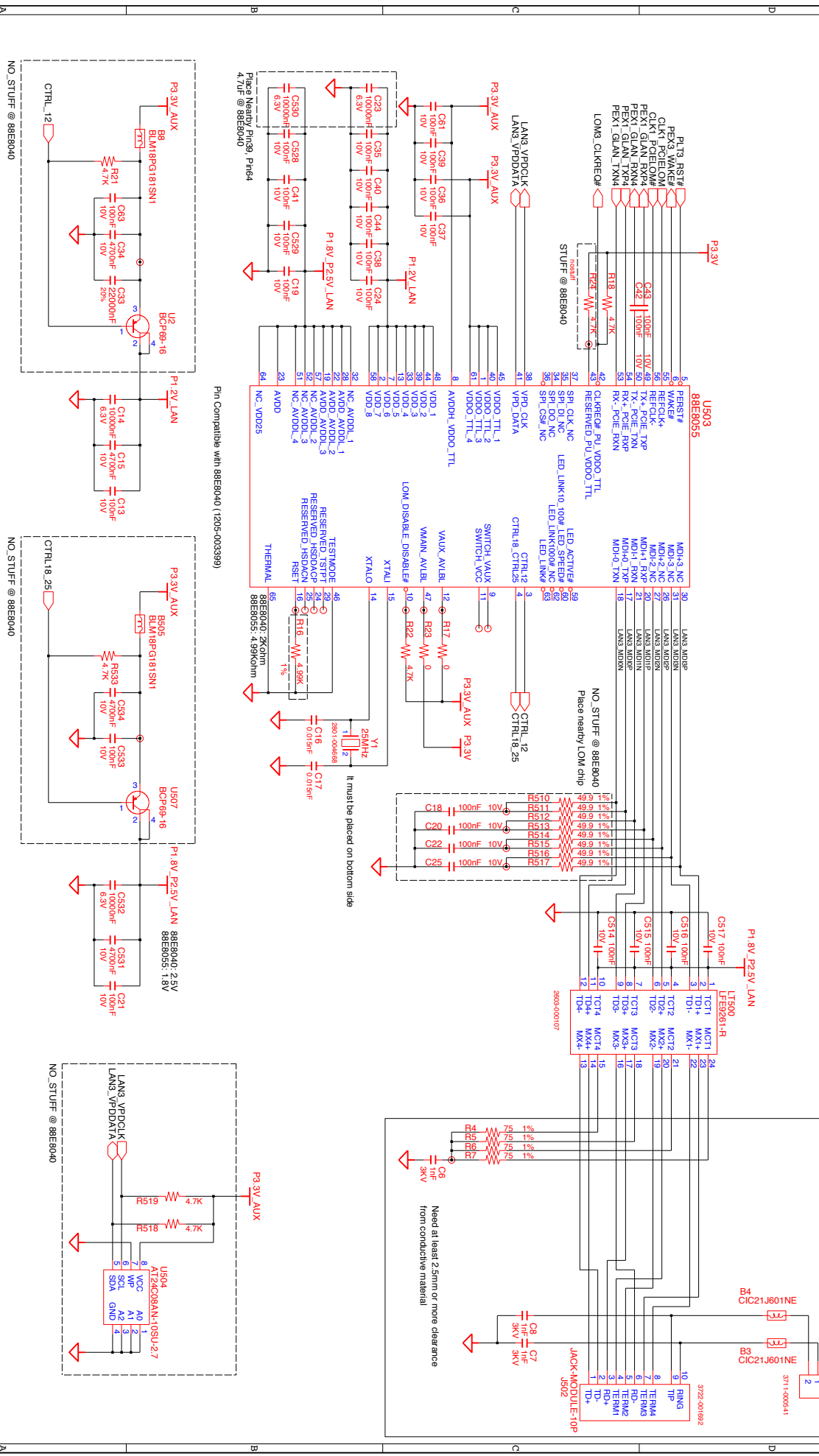


COM-22C-015(1996.6.5) REV. 3

COM-22C-015(1996.6.5) REV. 3

[illegible]

DATE	DATE	TITLE	SAMSUNG ELECTRONICS	
ORDER	TERMI	1/10/2008		
QUANTITY	REV. STEP	NP		
APPROVAL	REV	1.0		
PRODUCT CODE	LAST EDIT	June 09, 2008 11:54:01 AM		
2 in 1 Socket			PART NO.	BA-1-00920A
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REV	DATE	DESCRIPTION	BY	CHK
1.0	1/10/2008	LYON_External	HU KIM	MP
1.0	1/10/2008	MAIN	SJ PARK	REV
1.0	1/10/2008	LAN	LSF EDIT	ROUTE CODE

Switched Power On (P5.0V)

The diagram illustrates the power distribution network for the P5.0V supply. The power originates from the PMWON pin (P3.0V PMWON) and is distributed through a series of components:

- PMWON Pin:** P3.0V PMWON
- Resistor:** SHORT514 (0 Ohms)
- Capacitor:** C832 (100nF, 10V, ROSEHILL)
- Resistor:** R802 (30.1K, 1%)
- Capacitor:** C853 (100nF, 10V)
- IC:** O535 (AP4455GM, 5-pin package)
- Capacitor:** C854 (2200nF, 10V)
- Resistor:** R808 (0 Ohms)
- Resistor:** R809 (0 Ohms)
- Capacitor:** C851 (100nF)
- Capacitor:** C506 (100nF, 10V)
- Capacitor:** C512 (100nF, 10V)
- Capacitor:** C509 (100nF)
- Capacitor:** C507 (100nF)
- Capacitor:** C523 (100nF, 10V)
- Capacitor:** C508 (100nF)
- Capacitor:** C504 (100nF)
- Capacitor:** C800 (100nF)
- Capacitor:** C511 (100nF)
- Capacitor:** C505 (100nF)
- Capacitor:** C510 (100nF)
- Capacitor:** C503 (100nF)
- Capacitor:** C502 (100nF)
- Capacitor:** C501 (100nF)
- Capacitor:** C500 (100nF)
- Capacitor:** C509 (100nF)
- Capacitor:** C507 (100nF)
- Capacitor:** C523 (100nF, 10V)
- Capacitor:** C512 (100nF, 10V)
- Capacitor:** C506 (100nF, 10V)
- Capacitor:** C508 (100nF)
- Capacitor:** C504 (100nF)
- Capacitor:** C800 (100nF)
- Capacitor:** C511 (100nF)
- Capacitor:** C505 (100nF)
- Capacitor:** C510 (100nF)
- Capacitor:** C503 (100nF)
- Capacitor:** C502 (100nF)
- Capacitor:** C501 (100nF)
- Capacitor:** C500 (100nF)

The diagram also shows the connection of the P5.0V supply to various auxiliary USB ports (P5.0V AUX USB) and the P5.0V AUX pin.

[illegible]

Figure 10 shows four circuit diagrams for the P5_0V_AUX pin, each with a different input voltage (P3_0V_AUX, P5_0V_AUX, P5_0V_AUX, P5_0V_AUX). Each diagram includes a capacitor (C893, C894, C895, C896) connected to the P5_0V_AUX pin, with a 100nF capacitor and a 10V voltage source in parallel. The input voltages are P3_0V_AUX, P5_0V_AUX, P5_0V_AUX, and P5_0V_AUX respectively.

[illegible]

Diagram of the power supply section of the TDA1564Q. The circuit includes a transformer with a 50V primary and two 500V secondary windings. The primary is connected to a 470K resistor (R278) and a 200K resistor (R801). The secondary windings are connected to a 50V capacitor (C830) and a 2200µF capacitor (C864). The circuit includes two diodes (D29 and D28) and two integrated circuits (RHU02N06 and AP6880AGM). The output is connected to a 3.3V AUX terminal. A note indicates to place the 50V capacitor near the transformer.

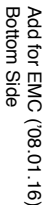
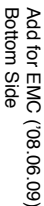
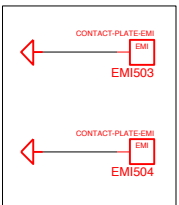
Diagram of the power supply section of the TDA1564Q. The circuit includes a transformer with a 50V primary and two 500V secondary windings. The primary is connected to a 470K resistor (R278) and a 200K resistor (R801). The secondary windings are connected to a 50V capacitor (C830) and a 2200µF capacitor (C864). The circuit includes two diodes (D29 and D28) and two integrated circuits (RHU02N06 and AP6880AGM). The output is connected to a 3.3V AUX terminal. A note indicates to place the 50V capacitor near the transformer.

Place near to

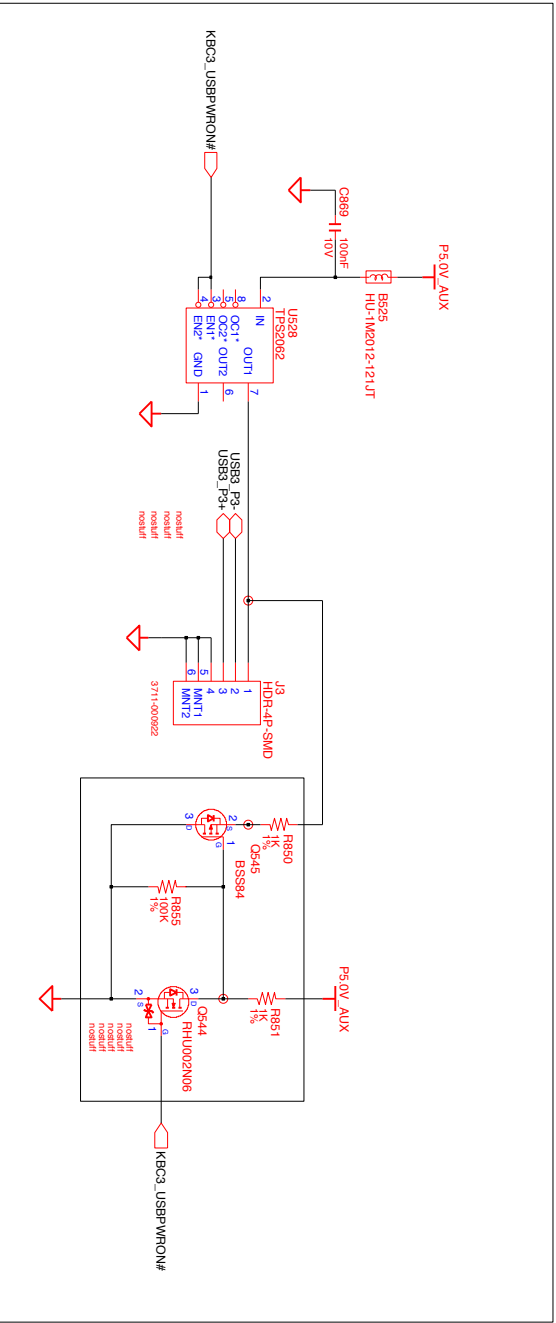
Figure 1 shows the schematic representation of 16 different EGFR constructs. The constructs are arranged in two columns. The left column contains: P1.1V, C889, P1.1V, C890, P1.1V, C891, P1.1V, C892, P1.1V, C895, P1.1V, C896, P1.1V, C897, and P1.1V, C898. The right column contains: P1.1V, C878, P1.1V, C879, P1.1V, C880, P1.8V, C881, P1.8V, C882, P1.8V, C883, P1.8V, C884, and P1.8V, C885. Each construct is represented by a schematic of the EGFR protein with a specific mutation highlighted in a colored box. The mutations are: C889 (red), C890 (blue), C891 (green), C892 (red), C895 (blue), C896 (green), C897 (red), C898 (blue), C878 (red), C879 (blue), C880 (green), C881 (red), C882 (blue), C883 (green), C884 (red), and C885 (blue).

COM-2020-01517-1996.6.5-REV. 3

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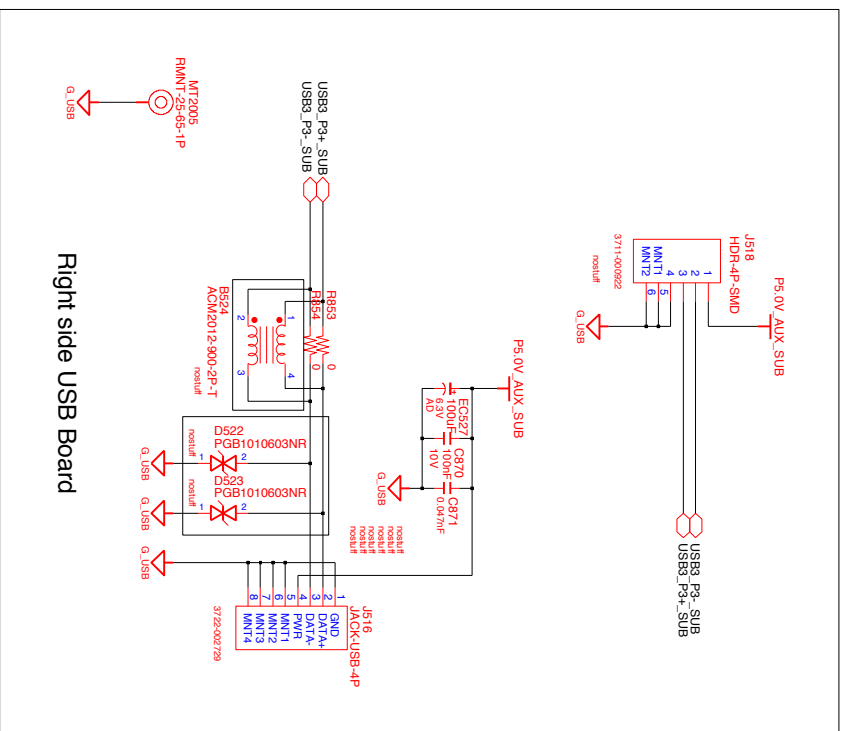
www.vinafix.vn



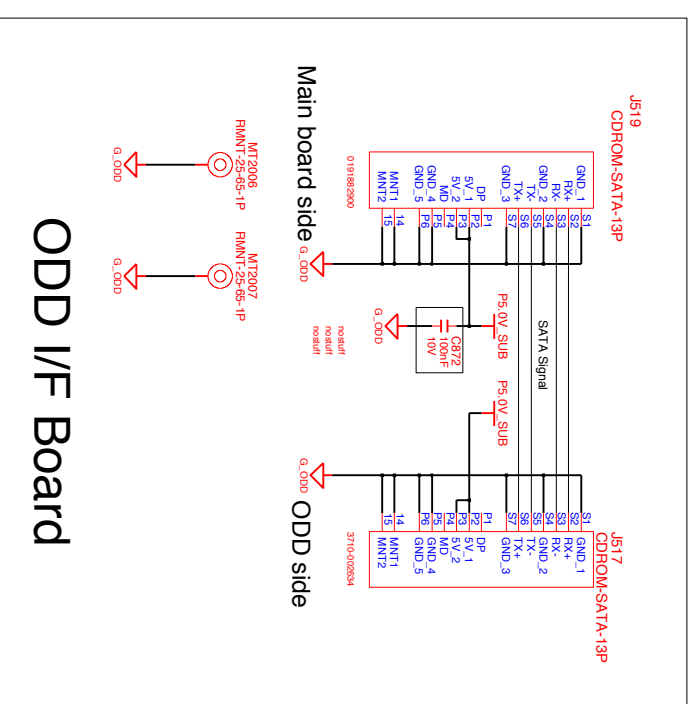
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2	1-2		
3	2-3		
4	3-1		
5	1-2-3		
6	N.C.		
7	1-2		
8	2-3		
9	3-1		
10	1-2-3		

DATE	DATE	TITLE	SAMSUNG ELECTRONICS
CHECK	TERMIN	1/10/2008	
APPROVAL	HU KIM	NP	
	REV	1.0	
MODEL CODE	SJ PARK	TP	
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Sub Board (Istanbul only)



Right side USB Board

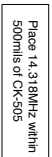


ODD I/F Board

DESIGN	TERM1	DATE	TITLE	SAMSUNG
CHECK	HU KIM	3/28/2008	LYON_External	ELECTRONICS
APPROVAL	SJ PARK	REV	SUB BOARD	
ROUTE CODE	1.0	REV	USB, ODD	
		LAST EDIT		
		June 09, 2008 11:54:01 AM		
		PAGE	18	OF 19

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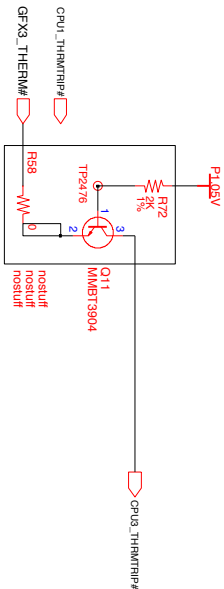
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APPROVAL	REV. STEP	MP	
MODIFY CODE	REV	1.0	
	LAST EDIT	June 09, 2008 11:54:01 AM	
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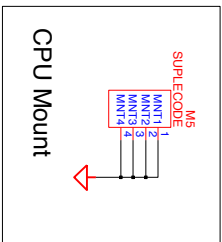
SEL_LCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SFC_0/SFC_0#	27M & 27M_SS

This part is 64pin QFN package.

REV	DATE	TITLE	SAMSUNG ELECTRONICS		
TERMI	1/10/2008	L YON - External	PART NO.	BA-11-00920A	
CHECK	REV: SGP	Main, Clock-Circuit			
APPROVAL	REV	CK-Clock-505M			
MODULE CODE	1.0				
undef: need	DATE EDIT	June 09, 2008 11:51:01 AM	PAGE	21	OF 64



DATE	DATE	TITLE	SAMSUNG		ELECTRONICS	
CHECK	TERMI	1/10/2008	L_YON_External			
APPROVAL	HU KIM	DEV. STP	thermal_Sensor_SMSC_Enc2102			
	SJ PARK	REV	thermal_Sensor_SMSC_Enc2102		PART NO.	BA411-000920A
MODEL CODE		LAST EDIT	June 09, 2008 11:54:01 AM		PAGE	61 OF 64

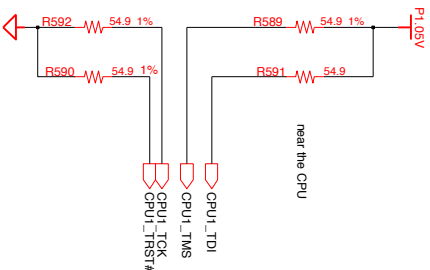


DATE		TITLE		SAMSUNG ELECTRONICS
ORDER	ITEM1	DATE SHIP	LYON-External	
APPROVAL	PL KIT	MP	CPU	
	SJ PARK	REV	PENRYN (1/3)	
ROUTE CODE	LAST EDIT			
under:ned		June 09, 2008 11:54:01 AM		PAGE 22 OF 64 PART NO. BA-1-00920A

CPU500-3
PENRYN
3 / 4

CPU Socket : 3704-001153

FSC	FSB	FSA	FRQ
0	0	0	266MHz
0	1	0	200MHz
0	1	1	166MHz



CPU Core Voltage Table IMV-P6

		Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
		Voltage	VID(e0)	Voltage	VID(e0)	Voltage	VID(e0)
Active DPRSL_PVR 0 DPRSTP* 1 PSIG* 0 or 1	VID(e0)	0	0	0	0	1	0
		1.4875 V	0	1	0	1	0
		1.475 V	0	1	0	1	0
		1.4625 V	0	1	0	1	0
		1.45 V	0	1	0	1	0
		1.4375 V	0	1	0	1	0
		1.425 V	0	1	0	1	0
		1.4125 V	0	1	0	1	0
		1.4 V	0	1	0	1	0
		1.3875 V	0	1	0	1	0
		1.375 V	0	1	0	1	0
		1.3625 V	0	1	0	1	0
		1.35 V	0	1	0	1	0
		1.3375 V	0	1	0	1	0
		1.325 V	0	1	0	1	0
Deeper Sp DPRSL_PVR 1 DPRSTP* 0 PSIG* 0 or 1	VID(e0)	1	0	1	0	1	0
		1.0000 V	1	0	1	0	1
		0.9875 V	1	0	1	0	1
		0.975 V	1	0	1	0	1
		0.9625 V	1	0	1	0	1
		0.95 V	1	0	1	0	1
		0.9375 V	1	0	1	0	1
		0.925 V	1	0	1	0	1
		0.9125 V	1	0	1	0	1
		0.9 V	1	0	1	0	1
		0.8875 V	1	0	1	0	1
		0.875 V	1	0	1	0	1
		0.8625 V	1	0	1	0	1
		0.85 V	1	0	1	0	1
		0.8375 V	1	0	1	0	1
		0.825 V	1	0	1	0	1
11111111 : 0V power good asserted.	VID(e0)	1	0	1	0	1	0
		0.4875 V	1	0	1	0	1
		0.475 V	1	0	1	0	1
		0.4625 V	1	0	1	0	1
		0.45 V	1	0	1	0	1
		0.4375 V	1	0	1	0	1
		0.425 V	1	0	1	0	1
		0.4125 V	1	0	1	0	1
		0.4 V	1	0	1	0	1
		0.3875 V	1	0	1	0	1
		0.375 V	1	0	1	0	1
		0.3625 V	1	0	1	0	1
		0.35 V	1	0	1	0	1
		0.3375 V	1	0	1	0	1
		0.325 V	1	0	1	0	1
		0.3125 V	1	0	1	0	1

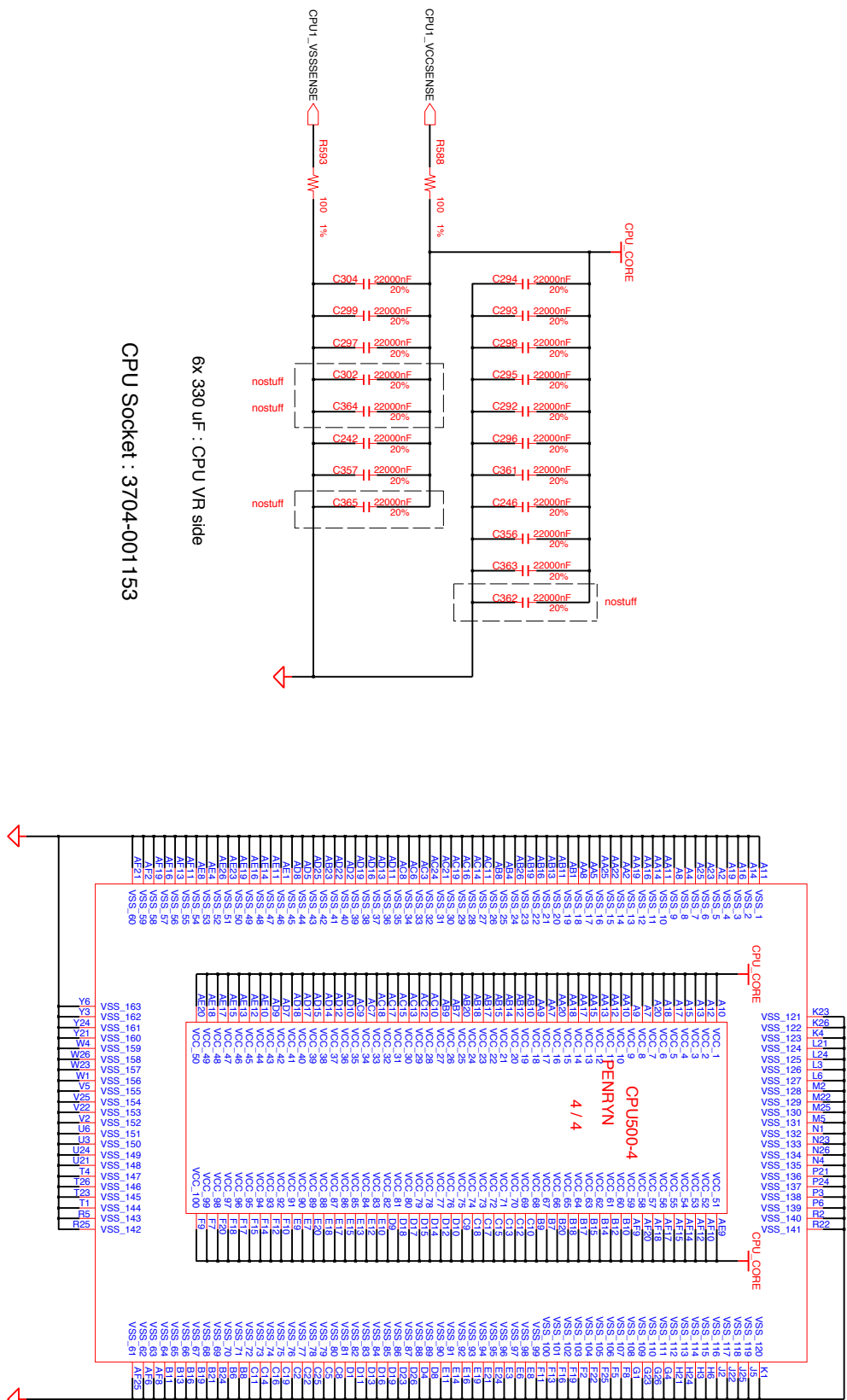
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTTLREF: Keep the Voltage divider within 0.5"
0.1 Ohm or less. Do not use 0.25 Ohm resistors.
Minimize coupling of any switching signals to this net.

COMFQ2/COMF1_3: should be connected with Zo=Z740m(55ohm)
Trace shorter than 1/2" to their respective Bannas socket pins.

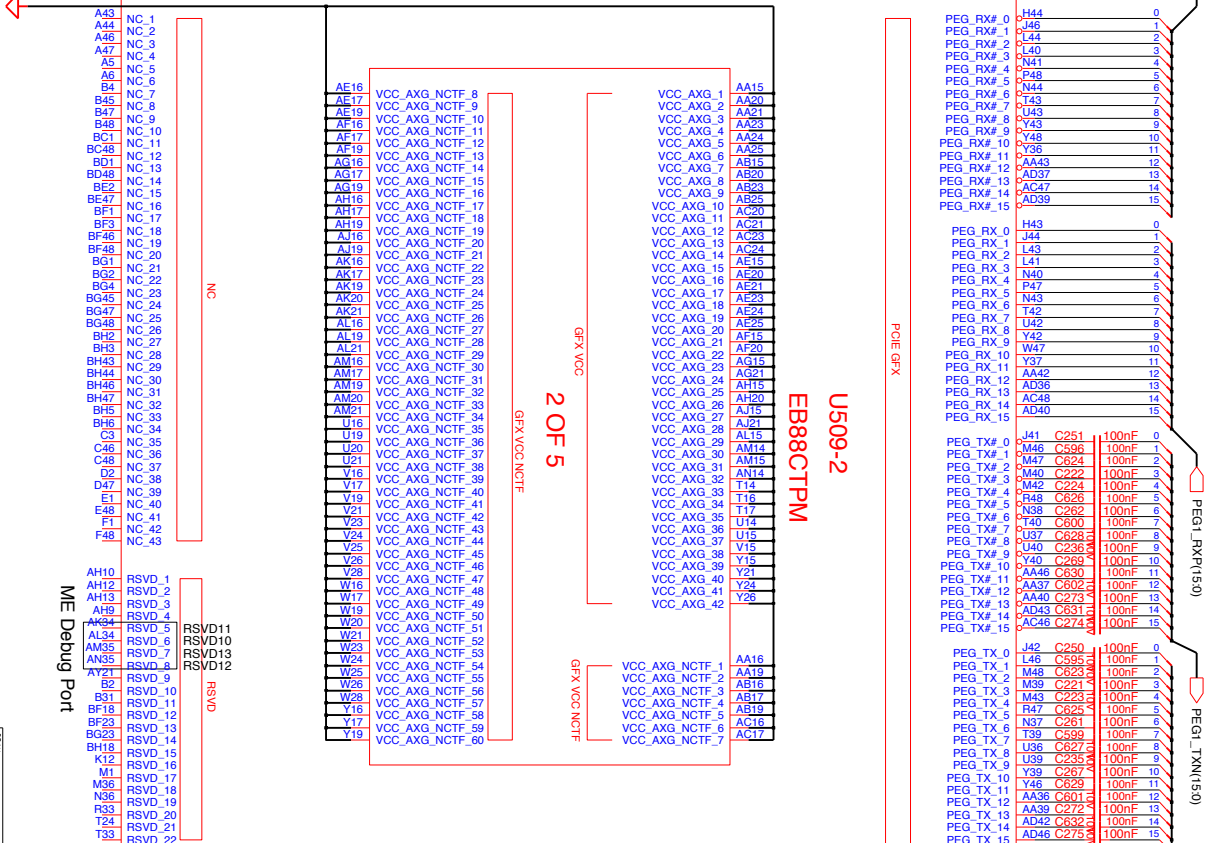
GND test points within 100mil of the VCC/VSSense at the end of the line.
Route the VCC/VSSense as a Z-axis trace as much as equal length.
Do not use 3-4 layer board. VCC/VSSense lines and 25mil away.
(Preferred signal) from any other signal. And GND via 100mil away
from each of the VCC/VSS test point vias.

RAW	TERM1	DATE	TITLE	SAMSUNG
DECK	HU KIM	REV. STEP	LYON_External CPU	ELECTRONICS
APPROVAL	SJ PARK	REV	PENRYN (2/3)	BA41-00920A
ROUTE CODE	undef ined	LAST EDIT	June 09, 2008 11:54:01 AM	PAGE 23 OF 64



REV	DATE	TITLE	SAMSUNG
001	1/10/2008	LYON_External	ELECTRONICS
002	REV. STEP	CPU	
003	REV	PENRYN (3/3)	
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005	REV	undef ined	
006	REV	June 09, 2008 11:54:01 AM	
007	REV	PAGE 24 OF 64	





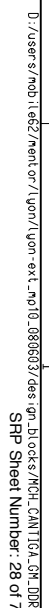
The schematic diagram illustrates the PEG105V power plane, showing various components and their connections. The diagram is organized into several functional blocks, each labeled with a color-coded header:

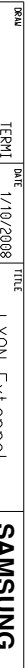
- PEG105V PEG** (Yellow header): The main power plane, connected to a 100V source. It includes a 100V source, a 100V source, and a 100V source.
- PEG COMPO** (Green header): Contains components like PEG105V, PEG105V, and PEG105V.
- CLK** (Blue header): Contains components like CLK1, CLK2, and CLK3.
- ME** (Blue header): Contains components like ME1, ME2, and ME3.
- PM** (Blue header): Contains components like PM1, PM2, and PM3.
- MISC** (Blue header): Contains components like MISC1, MISC2, and MISC3.
- PCIe GFX** (Blue header): Contains components like PCIe1, PCIe2, and PCIe3.

The diagram shows a complex network of connections between these blocks, including various resistors, capacitors, and inductors. Key components include:

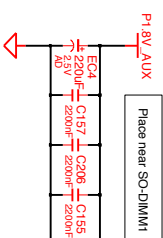
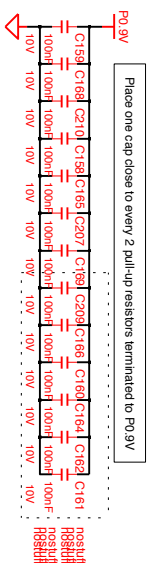
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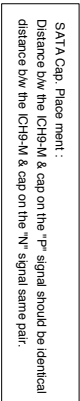


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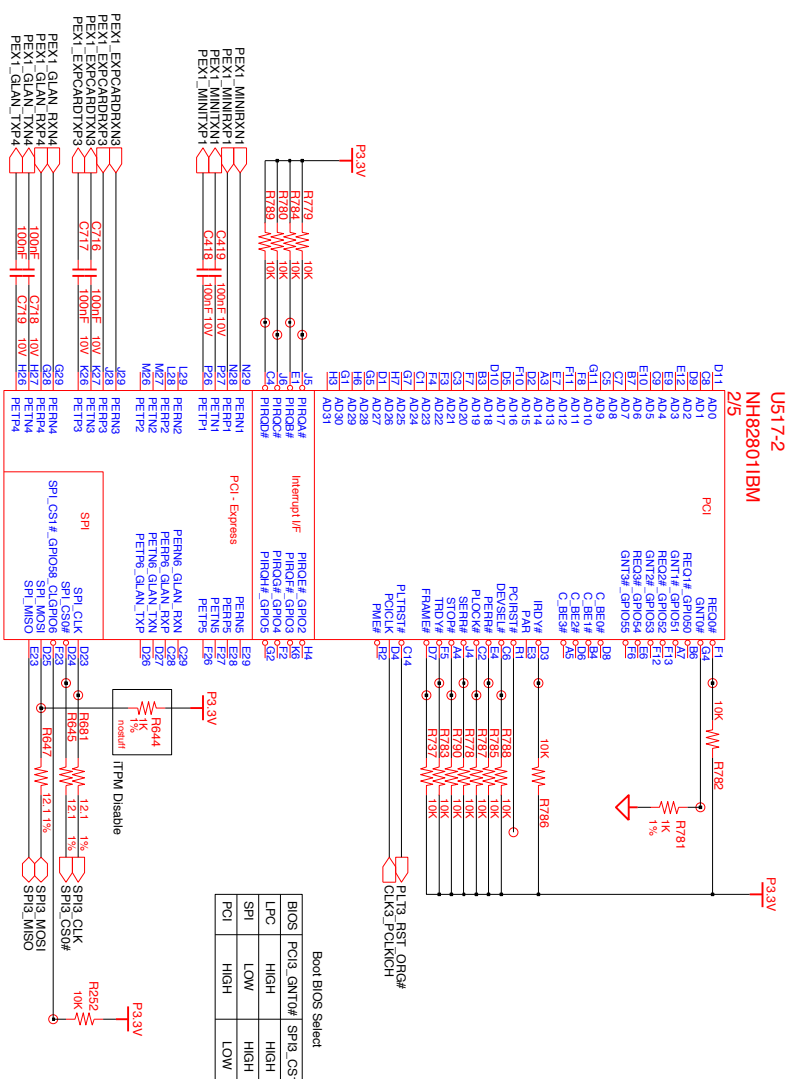
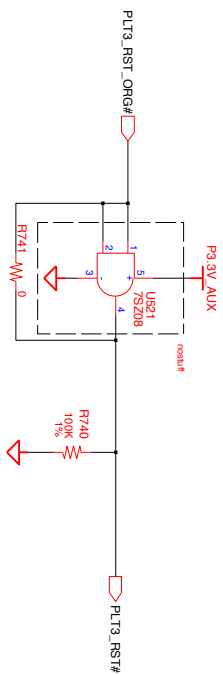


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ROULTE CODE	SJ PARK	REV	SOD1MM_D0R2 #2	
	LAST EDIT	1.0	PART NO.	BA-11-00920A
June 09, 2008 11:54:01 AM			PAGE	59 OF 64

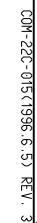
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VccSus1_05, VccSus1_5, VccCL1_5
VccLAN1_05, VccCL1_05

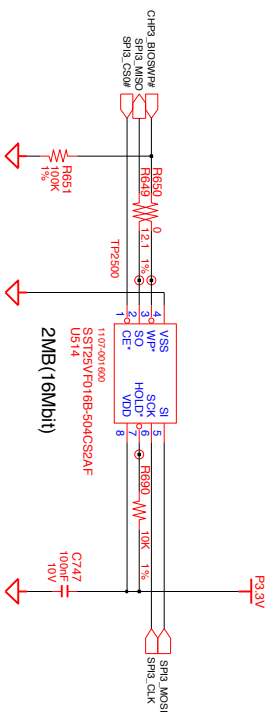


REV#	TITLE		SAMSUNG	
CHECK	TERM1	L YON_External		ELECTRONICS
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	REV	IC9H-M (1/5)	PART NO.	BA-1-00920A
MODIFY CODE	SJ PARK	1.0		
	LAST EDIT	June 09, 2008 11:54:01 AM		
		PAGE	34	OF 64

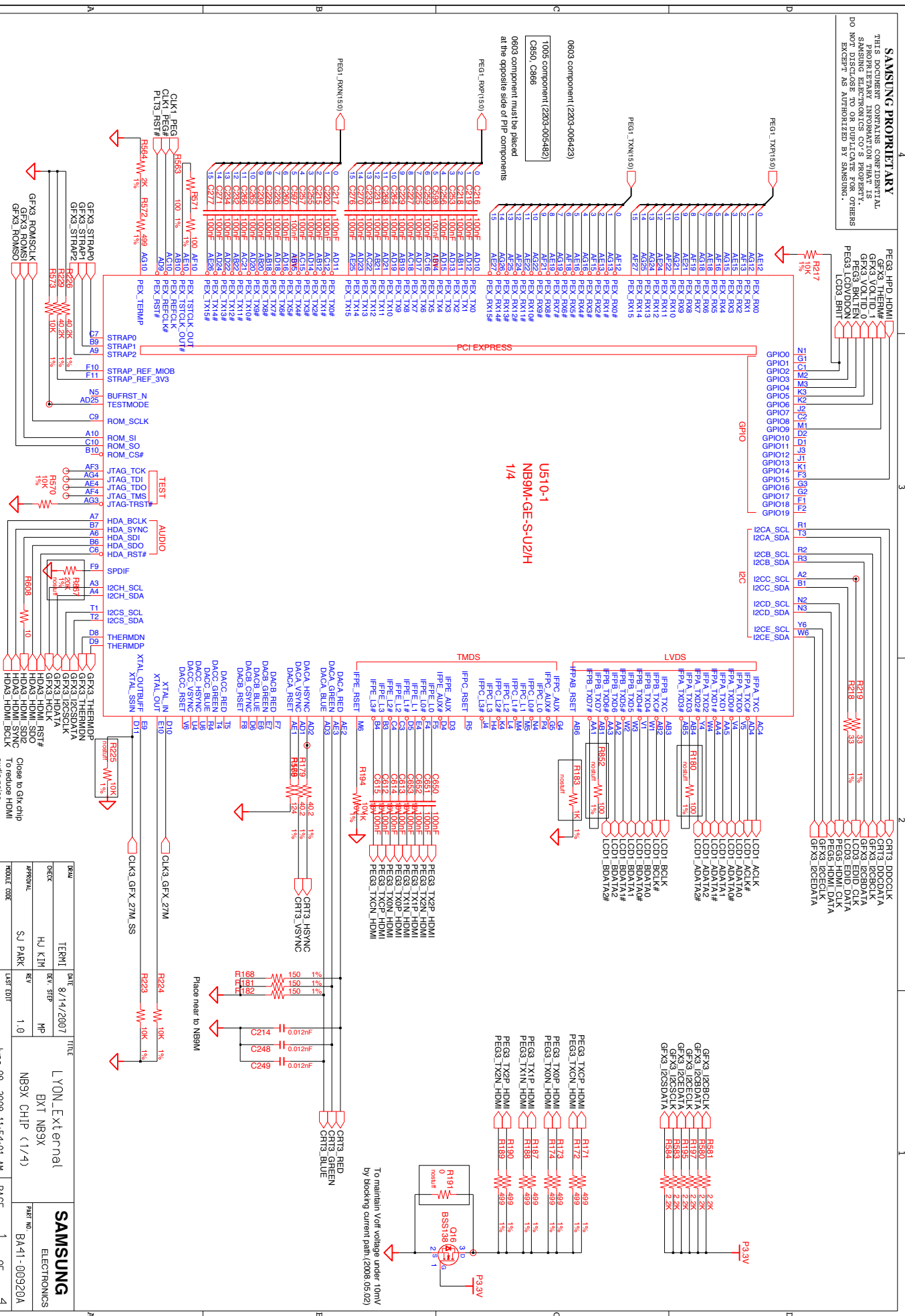


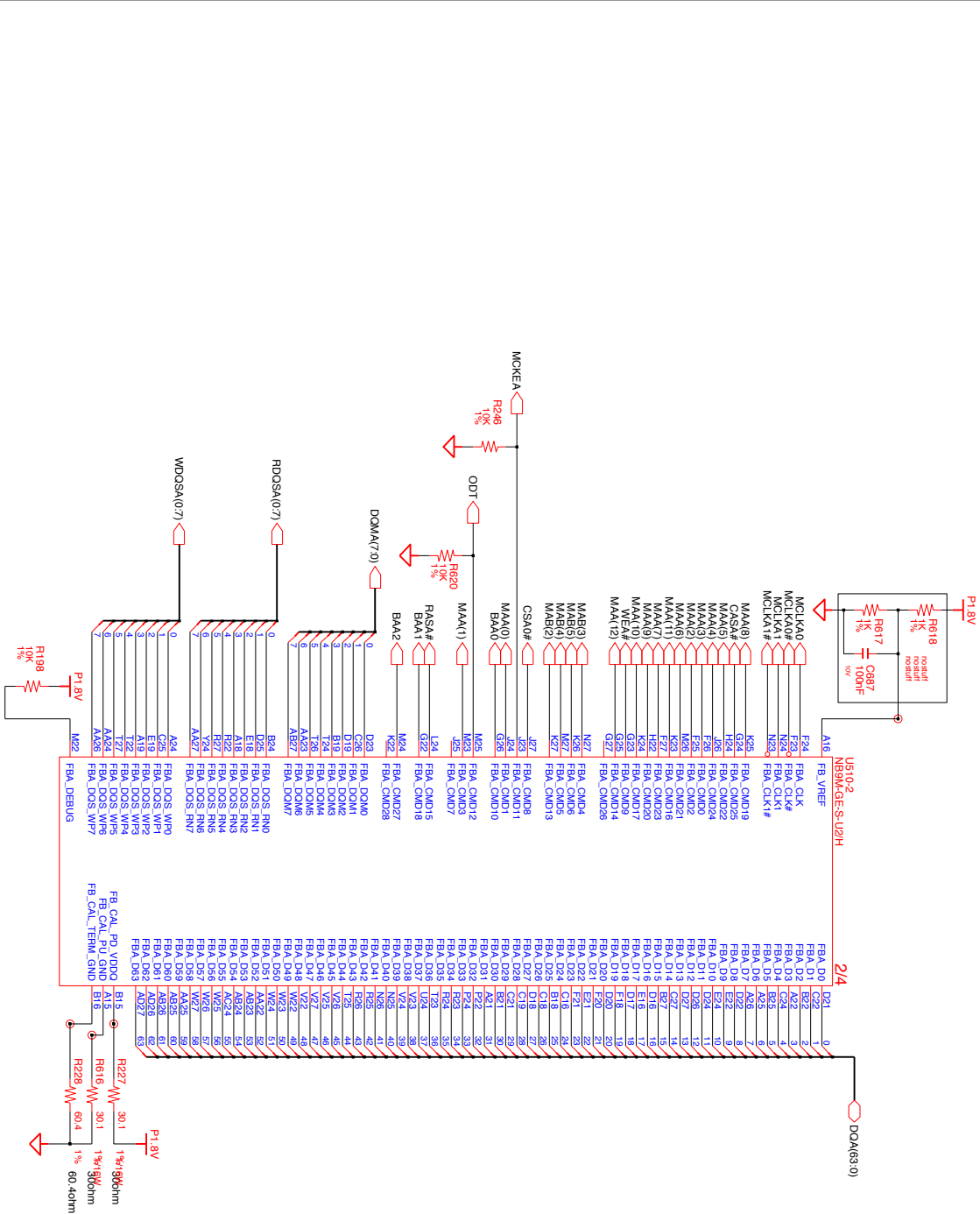
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APPROVAL	REV	ICH9-M (2/5)	
SJ PARK	1.0		BA41-00920A
ROUTE CODE	UNDEF EDIT	June 09, 2008 11:54:01 AM	PAGE 35 OF 64



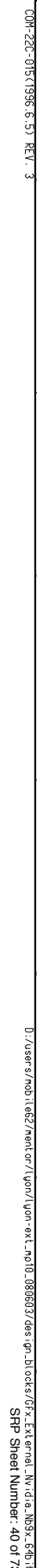
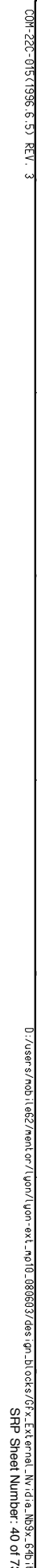


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM HW	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0E	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0F	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
10	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
11	LOAD ALTERNATE REG.	82	DETECT AND INSTALL EXT RS232C
13	PCI BUS MASTER RESET	84	DETECT AND INSTALL EXT PARALLEL
14	WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
16	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
18	CHECK CHECKSUM	8A	INIT. EXTENDED BIOS DATA AREA
1A	8254 TIMER INIT.	8C	INIT. FPD CONTROLLER
1C	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
20	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
22	TEST DRAM REFRESH	9E	ENABLE HW INTERRUPT
24	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
26	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
28	ENABLE A20	A8	ERASE F2 PROMPT
2A	AUTO SIZING DRAM	AC	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AA	ENTER SETUP
34	TEST CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
42	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
44	INT. INTERRUPT VECTOR	B7	ACPI INIT
46	INT. BIOS INTERRUPT	BA	DMI INIT
48	CHECK ROM COPYRIGHT NOTICE	BC	CLEAR SCREEN
49	INT. 120 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
4A	INT. PCI BIOS AND DEVICE	D0	INTERRUPT HANDLER ERROR
4C	INIT. ALL VIDEO BIOS ROM	D2	UNKNOWN INTERRUPT ERROR
4E	SHADOW VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
50	DISPLAY CPU TYPE AND SPEED	D6	SHUTDOWN 5
52	TEST KEYBOARD	D8	SHUTDOWN ERROR
54	SET KEYCLICK IF ENABLED	DA	EXTENDED BLOCK MOVE
56	ENABLE KEYBOARD	DC	SHUTDOWN 10
58	TEST FOR UNEXPECTED INTERRUPTS	DE	ENABLE NMI
5A	DISPLAY "PRESS SETUP"	80	INIT. HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	90	INIT. LOCAL BUS HDD CONTROLLER
60	TEST EXTENDED MEMORY	92	JUMP TO USER PATCH 2
62	TEST EXTENDED MEMORY ADDRESS LINE	94	DISABLE A20 ADDRESS LINE
64	JUMP TO USER PATCH 1	96	CLEAR HUGE ES SEGMENT REG.
		98	SEARCH FOR OPTION ROMS





RAW	DATE	TITLE
TERM1	8/14/2007	L'YON_External
CHECK	HJ KIM REV. STEP MP	EXT NB9X
APPROVAL	SJ PARK REV 1.0	NB9X CHIP (Z/d)
MODULE CODE	USER EDIT	PART NO. BA-411-00920A
		JUNE 09, 2008 11:54:01 AM
		PAGE 2 OF 4



CONFIDENTIAL (1986.6.5) REV. 3

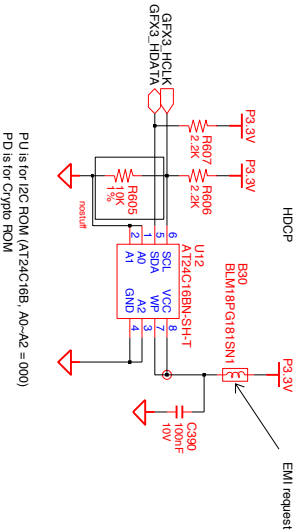
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SRP Sheet Number: 40 of 71

Pin	Description	Activate
GPIO0	DIV detect	High
GPIO1	TV detect	Low
GPIO2	PWM Brightness control	High
GPIO3	LCD VDD on enable	High
GPIO4	Backlight control	High
GPIO5	GPU VDD	High = 1.0V, Low = 1.1V
GPIO6	GPU VDD	NC
GPIO7	GPU VDD2 or Mem VDD	NC
GPIO8	Thermal detect Alert	LOW
GPIO9	Fan control	NC
GPIO10	Memory VREF switch	NC
GPIO11	SU Raster sync	HIGH
GPIO12	AC Power detection input	NC
GPIO13	Power supply control	NC
GPIO14	HDMI Detect	High
GPIO16	DP Detect	High

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_S0	XCLK27	TWODEE2	TWODEE1	TWODEE0
ROM_SCLK	DEVID4	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG3	RAMCFG2	RAMCFG1	RAMCFG0
STRAP2	DEVID3	DEVID2	DEVID1	DEVID0
STRAP1	PADCFG3	PADCFG2	PADCFG1	PADCFG0
STRAP0	USER9	USER12	USER11	USER10
Resistor value	PU to VDD	PU to GND	XCLK27 = 1.27MHz	
5K ohm	1000	0000	FAM_CFG (SEC)	
10 Kohm	1001	0001	0011 512Mbit 0111 1GBit	
15K ohm	1010	0010	USER10:0111169 EDD	
20K ohm	1011	0011	PADCFG3:0001 01NP	
25K ohm	1100	0101	NB9M-GS-0X06E9 (01001)	
30K ohm	1101	0101	NB9P-GS-0X0649 (01001)	
35K ohm	1110	0110	NB9P-GS-0X0406 (001110)	
45K ohm	1111	0111	NB9P-GS-0X0777 (077777)	

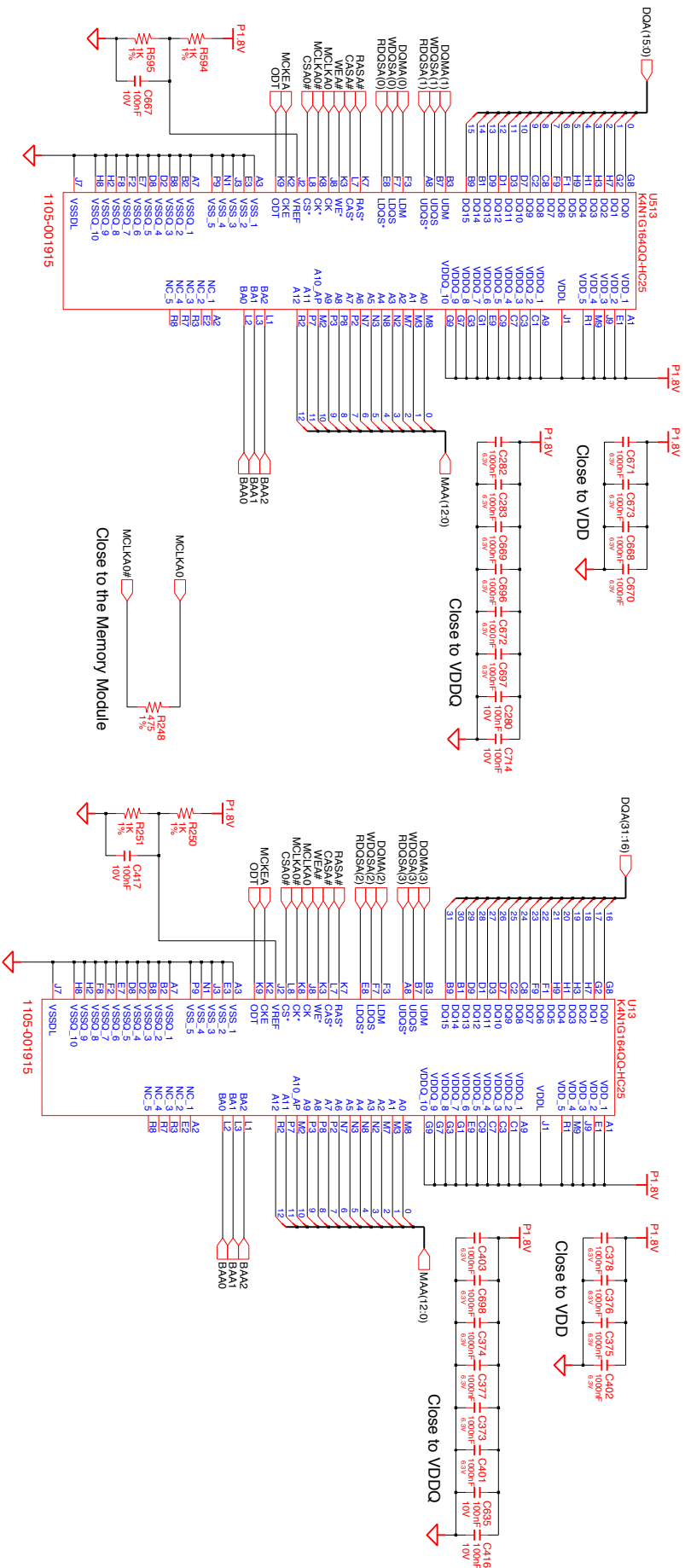
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B3	GND	U13	GND	U13
B4	GND	U14	GND	U14
B5	GND	U15	GND	U15
B6	GND	U16	GND	U16
B7	GND	U17	GND	U17
B8	GND	U18	GND	U18
B9	GND	U19	GND	U19
B10	GND	U20	GND	U20
B11	GND	U21	GND	U21
B12	GND	U22	GND	U22
B13	GND	U23	GND	U23
B14	GND	U24	GND	U24
B15	GND	U25	GND	U25
B16	GND	U26	GND	U26
B17	GND	U27	GND	U27
B18	GND	U28	GND	U28
B19	GND	U29	GND	U29
B20	GND	U30	GND	U30
B21	GND	U31	GND	U31
B22	GND	U32	GND	U32
B23	GND	U33	GND	U33
B24	GND	U34	GND	U34
B25	GND	U35	GND	U35
B26	GND	U36	GND	U36
B27	GND	U37	GND	U37
B28	GND	U38	GND	U38
B29	GND	U39	GND	U39
B30	GND	U40	GND	U40
B31	GND	U41	GND	U41
B32	GND	U42	GND	U42
B33	GND	U43	GND	U43
B34	GND	U44	GND	U44
B35	GND	U45	GND	U45
B36	GND	U46	GND	U46
B37	GND	U47	GND	U47
B38	GND	U48	GND	U48
B39	GND	U49	GND	U49
B40	GND	U50	GND	U50
B41	GND	U51	GND	U51
B42	GND	U52	GND	U52



GPIO2 Chip	Ra	Rb
GPIO2	noval	stiff
GPIO3	noval	stiff
GPIO4	noval	stiff

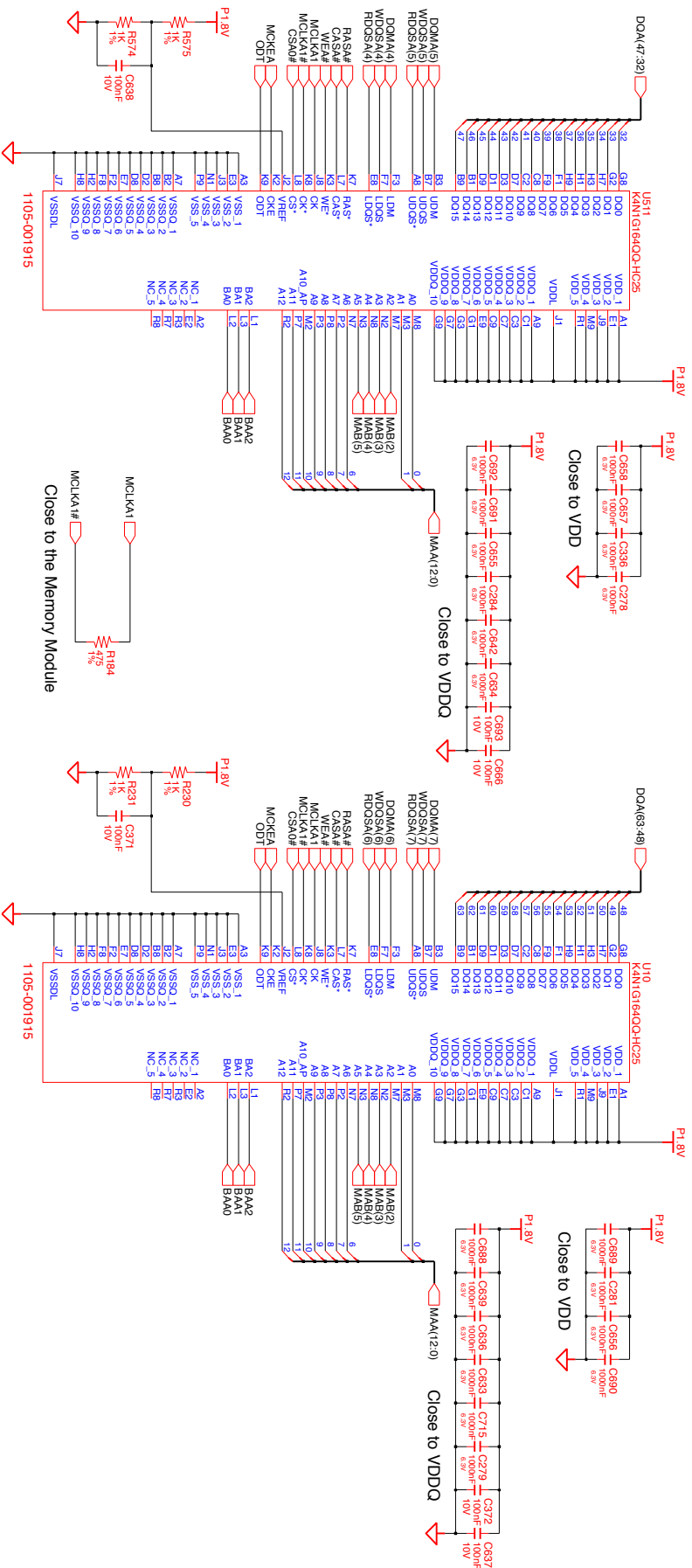
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EXT NB9X		
REV	MP	
APPROVAL	SJ PARK	
ROUTE CODE	LSF EDIT	
June 09, 2008 11:54:01 AM	PAGE 4	OF 4

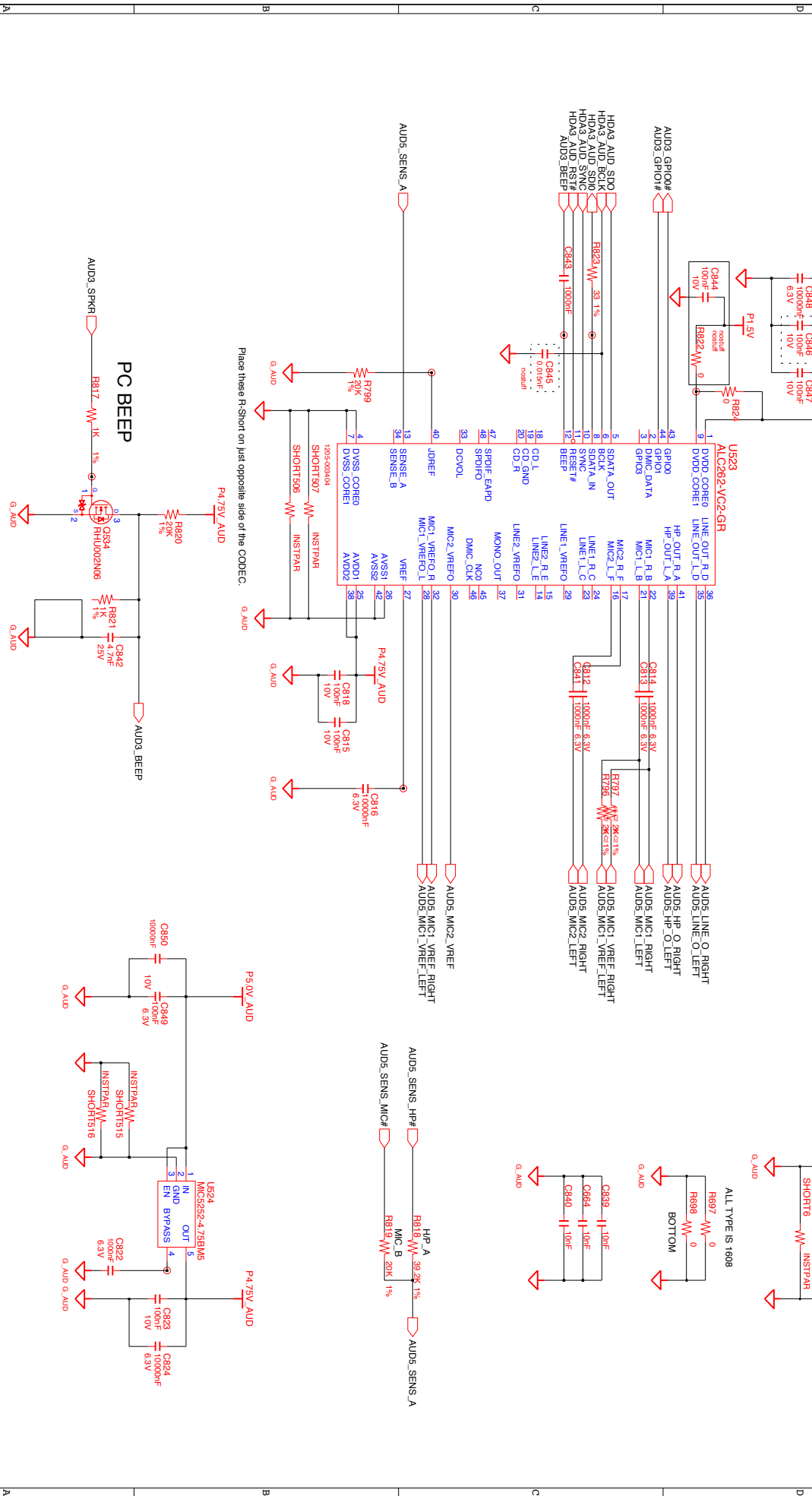
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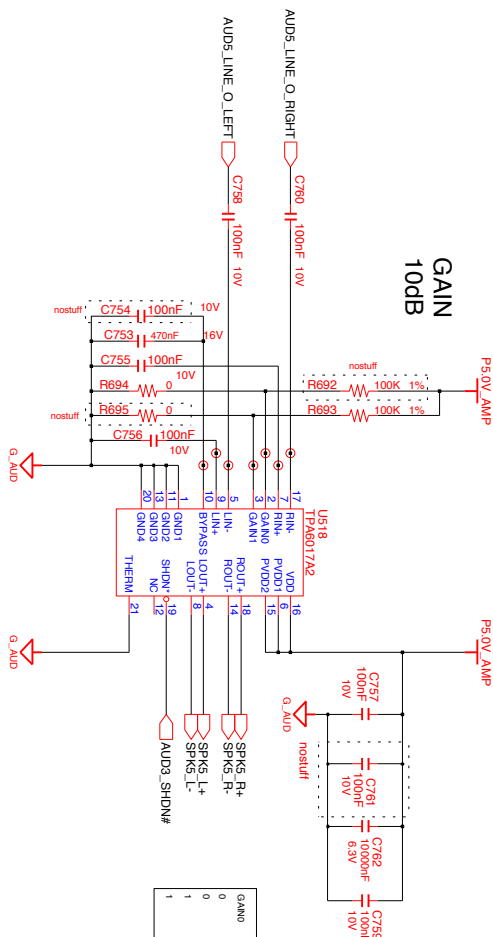
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002	REV. STEP	Graphics_Memory(GDDR2)	ELECTRONICS
003	REV	MP	
004	REV	SJ PARK	BA41-00920A
005	REV EDIT	June 09, 2008 11:54:01 AM	
006	ROUTE CODE		

UPPER SUB PARTITION

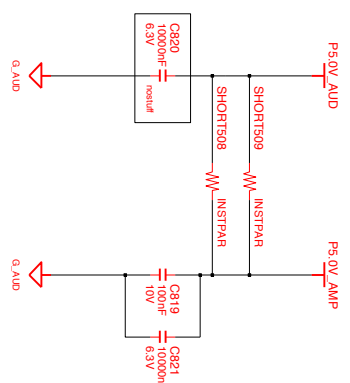




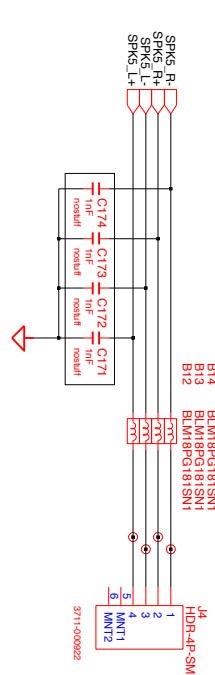
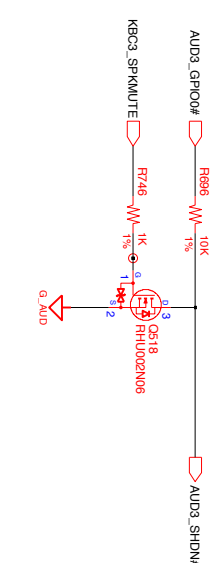
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MODULE CODE	LAST EDIT	PAGE 28	OF 64
undef med	June 09, 2008 11:54:01 AM		



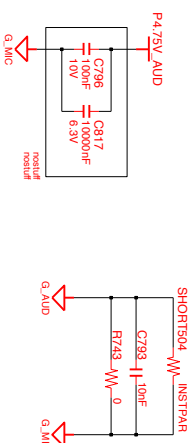
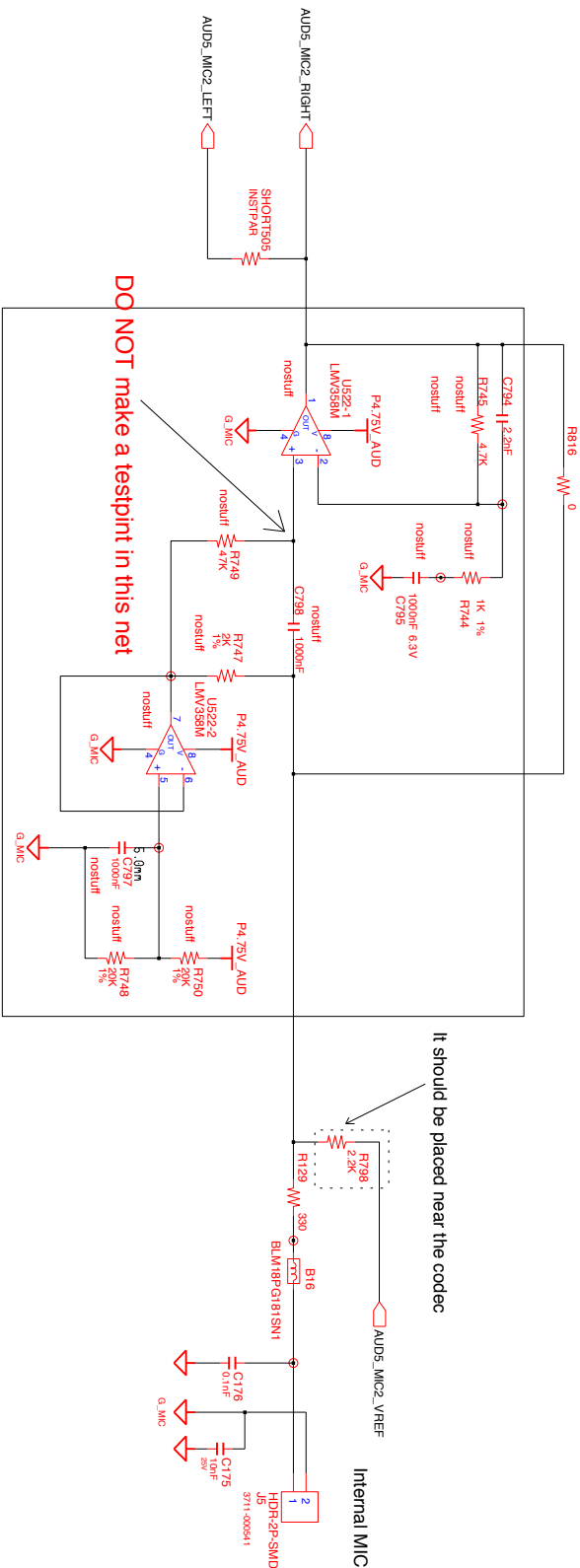
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R693	100K	1%
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R695	0	10V
R696	10K	1%
R746	1K	1%
C753	470nF	10V
C754	100nF	10V
C755	100nF	10V
C756	100nF	10V
C757	100nF	10V
C761	100nF	10V
C762	1000nF	6.3V
C759	100nF	10V



INTERNAL STEREO SPEAKERS

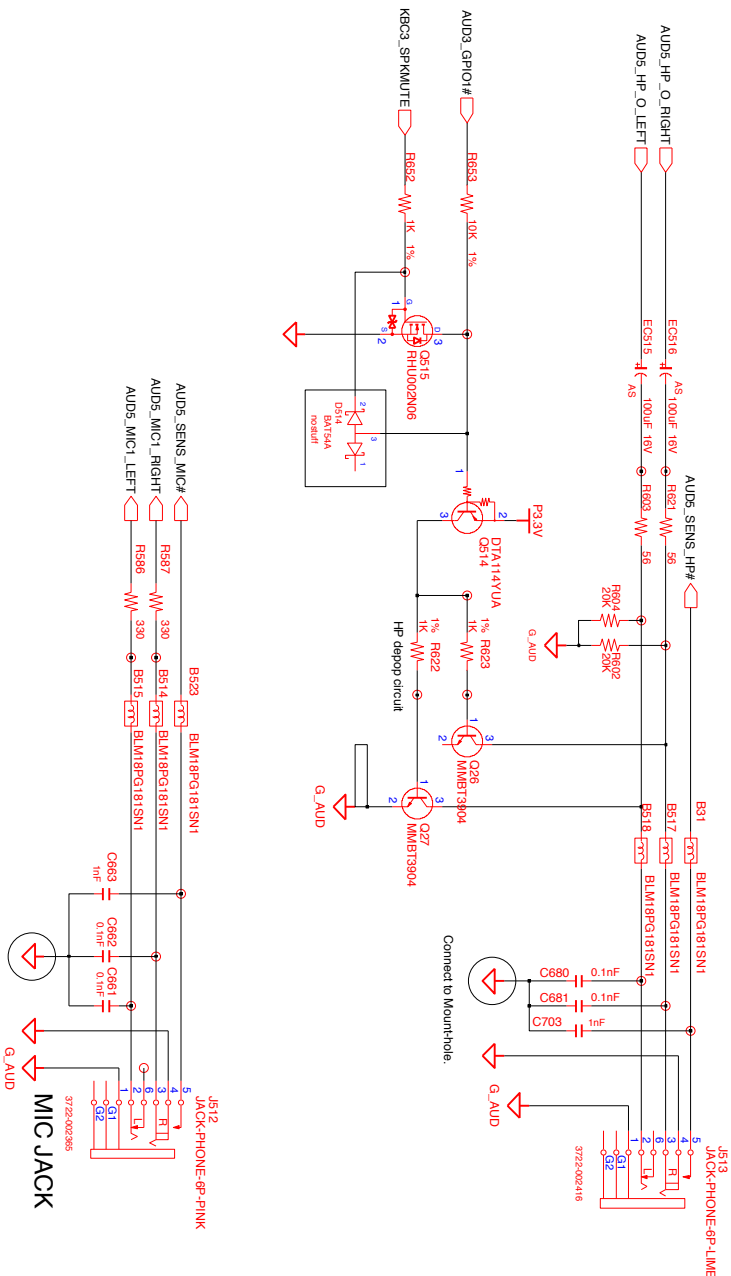


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4.0	1/10/2008	HDA_Codec-AIc262 #2	
5.0	1/10/2008	HDA_Codec-AIc262 #2	
6.0	1/10/2008	HDA_Codec-AIc262 #2	
7.0	1/10/2008	HDA_Codec-AIc262 #2	
8.0	1/10/2008	HDA_Codec-AIc262 #2	
9.0	1/10/2008	HDA_Codec-AIc262 #2	
10.0	1/10/2008	HDA_Codec-AIc262 #2	



REV	TERM	DATE	TITLE	SAMSUNG
0001	1/10/2008	LYON_External		
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0003	SJ PARK	REV	HDA_CODEC_AIC262 #3	
0004	undef:ned	LAST EDIT	June 09, 2008 11:54:01 AM	
0005		PAGE	30	OF 64

HEADPHONE



The traces led to Audio Jacks have the width over 10mil

RAW	TERM1	DATE	1/10/2008	TITLE	LYON_External
DECK	HJ KIM	REV. STEP	MP		HDA_Codec-AIC262
APPROVAL	SJ PARK	REV	1.0		HDA_Codec-AIC262_#4
ROUTE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	31 OF 64

SAMSUNG
ELECTRONICS

PART NO. BA41-00920A

4

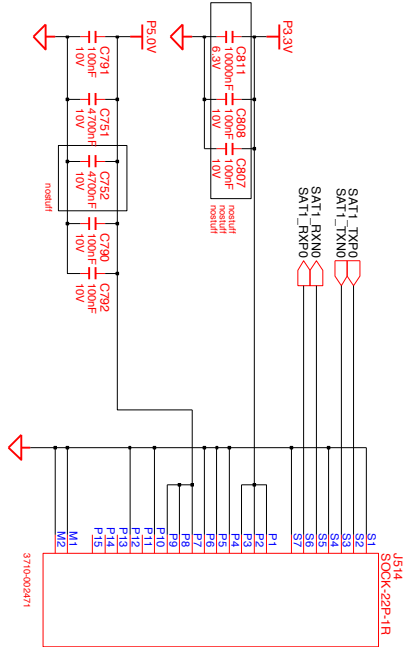


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11

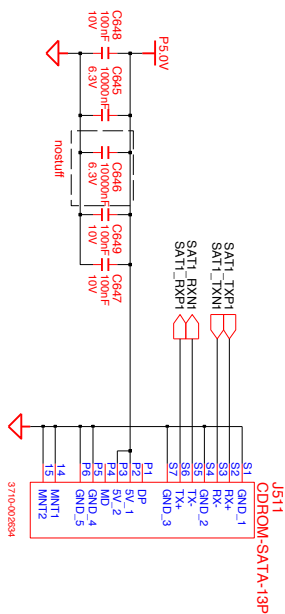
1

Main to HDD



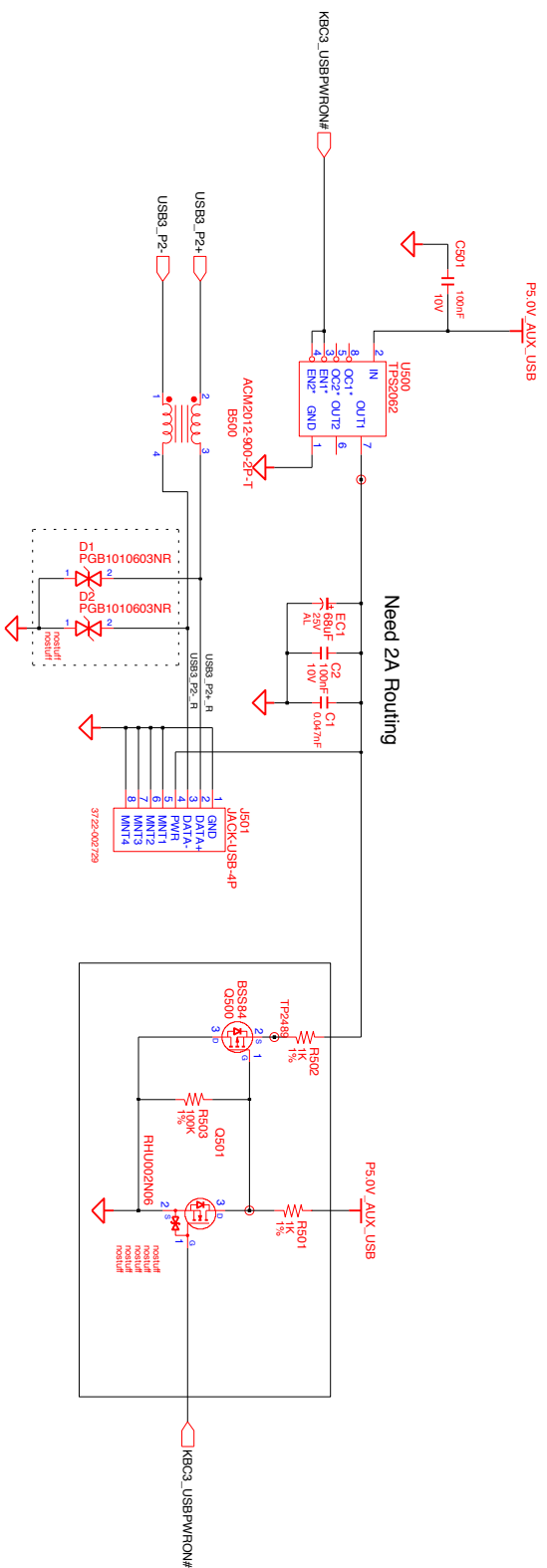
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ROUTE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	33	OF 64

SATA ODD



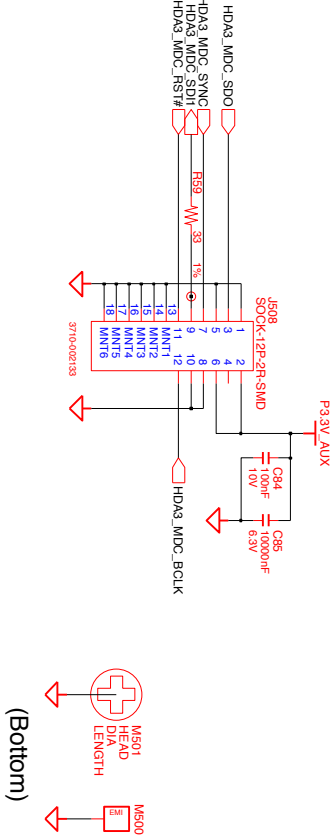
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ROUTE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	49 OF 64

1 PORT USB CONNECTOR



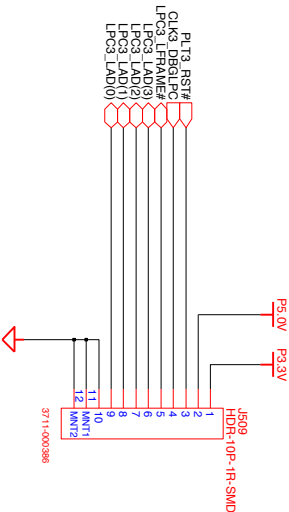
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ROUTE CODE	LSF EDIT	June 09, 2008 11:54:01 AM	PAGE 63 OF 64	

MDC Connector

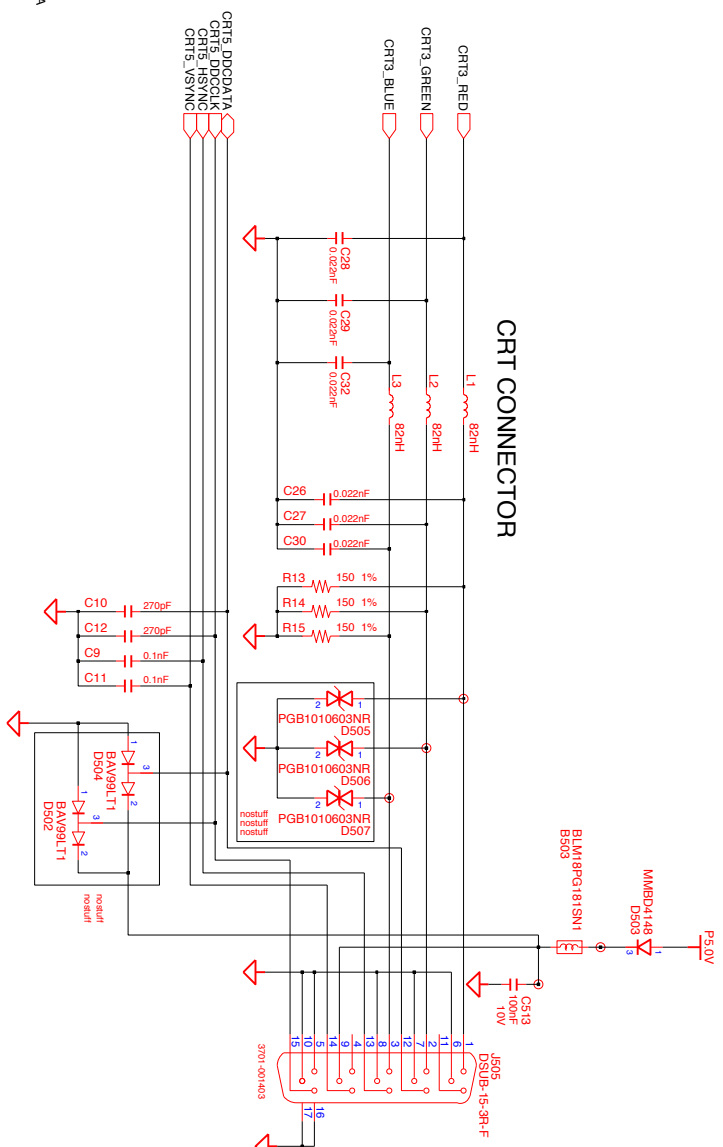
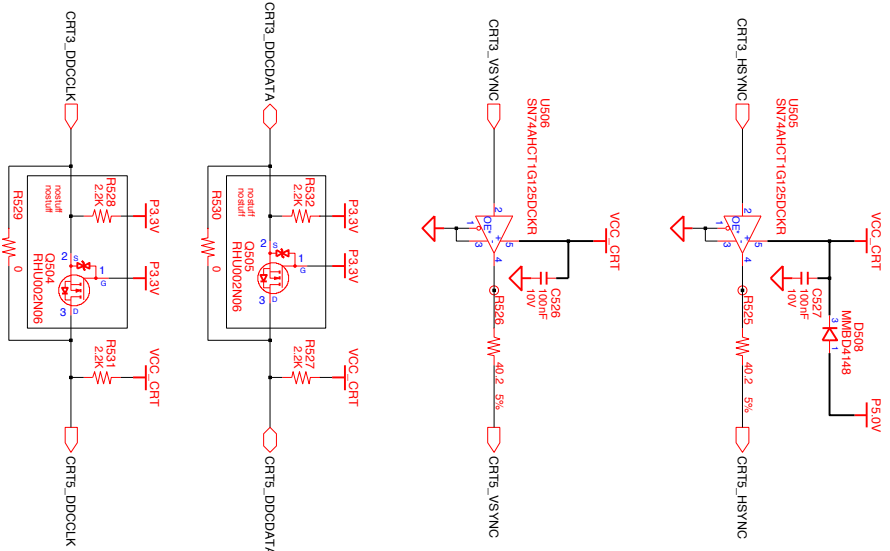


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ROUTE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	32	OF 64

80H DECODER CONNECTOR



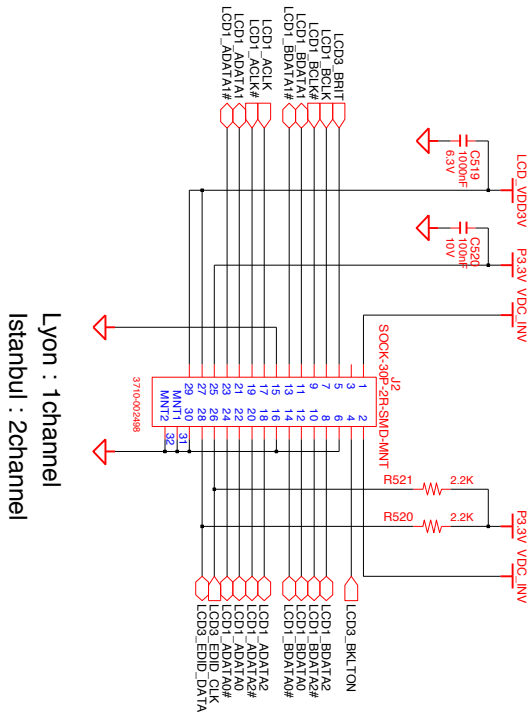
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ROUTE CODE	LSF EDIT	June 09, 2008 11:54:01 AM	Other_Debug-80	
		PAGE	50	OF 64



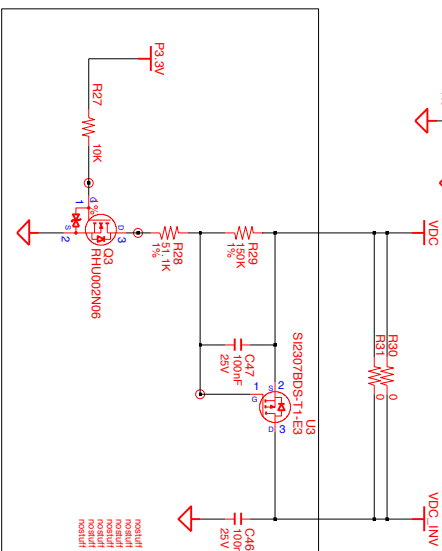
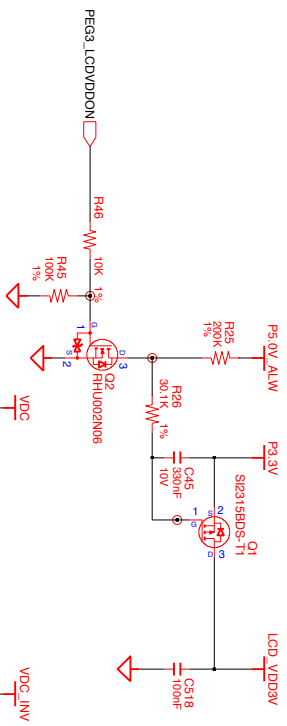
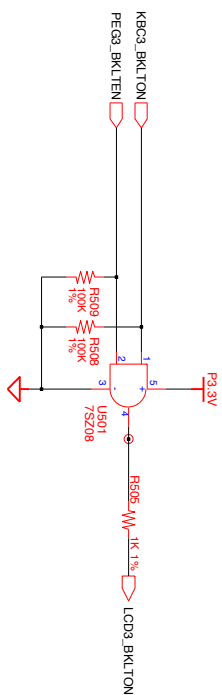
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DESIGNER	HU KIM	MP	Graphics-IF-CRT
REVISION	1.0	DATE	June 09, 2008 11:54:01 AM
ROUTE CODE	LSF EDIT	PAGE	25 OF 64

SAMSUNG
ELECTRONICS

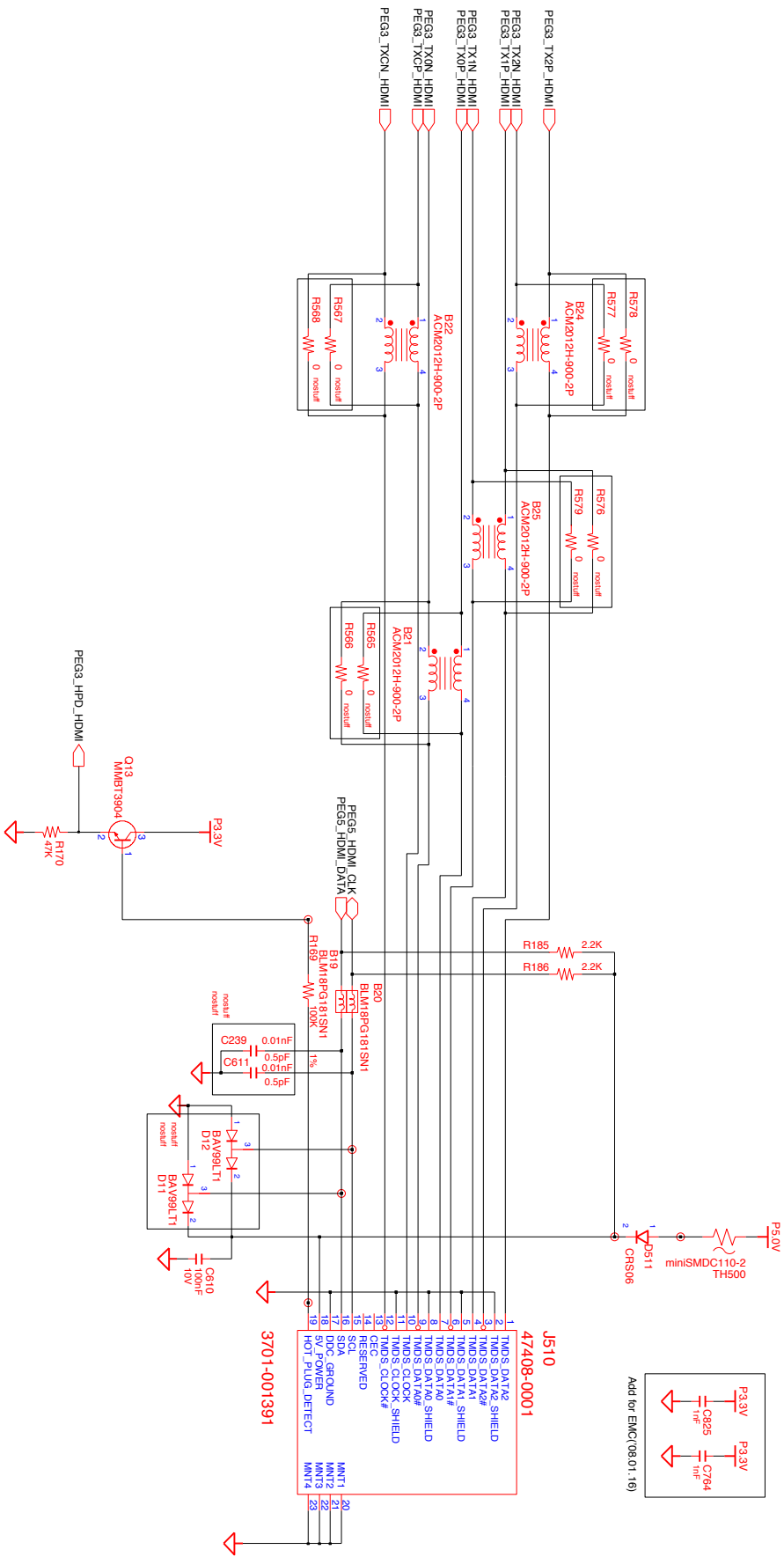
PART NO.
BA-41-00920A

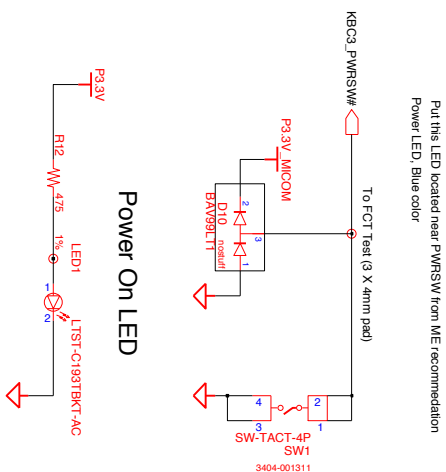


Lyon : 1channel
Istanbul : 2channel



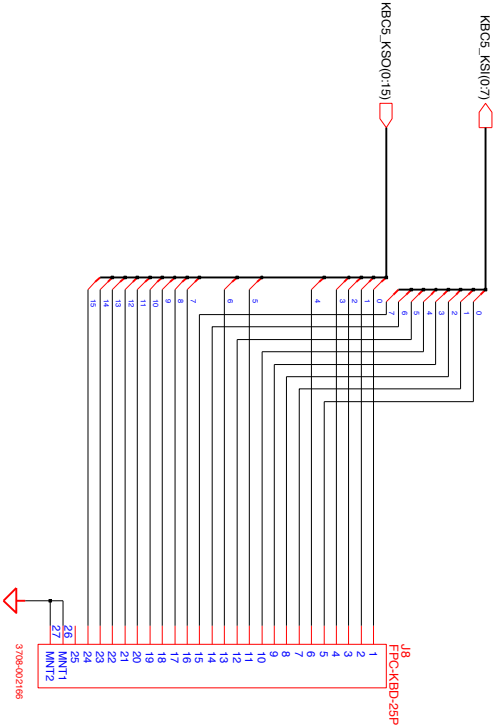
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004	LSF EDIT	June 09, 2008 11:54:01 AM	PAGE 12 of 73





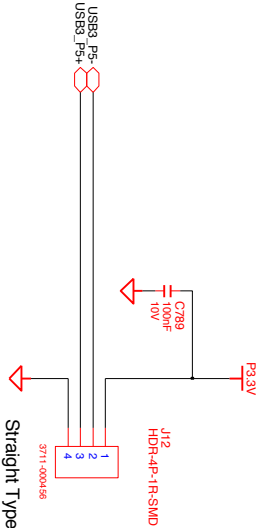
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KEYBOARD



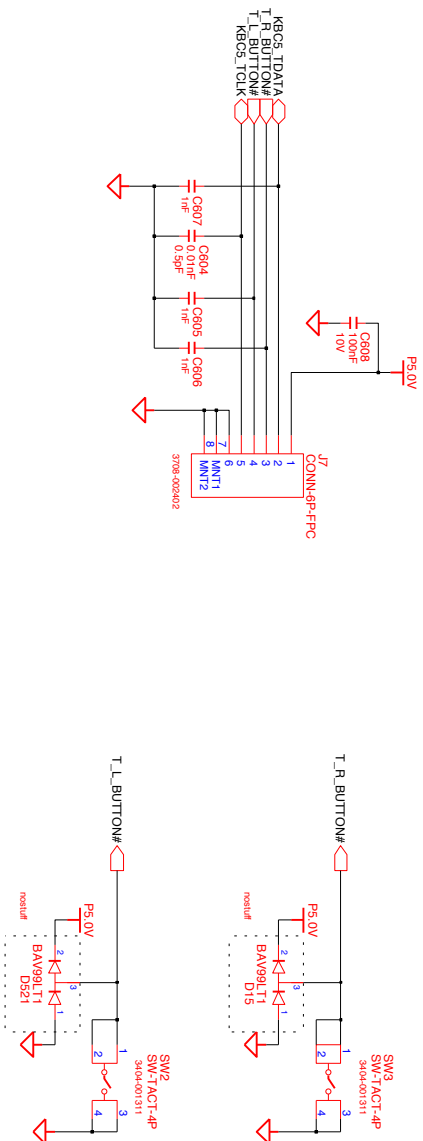
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0005		1/10/2008	KBD_IF_Conn	
0006		1/10/2008	KBD_IF_Conn	
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Bluetooth Interface



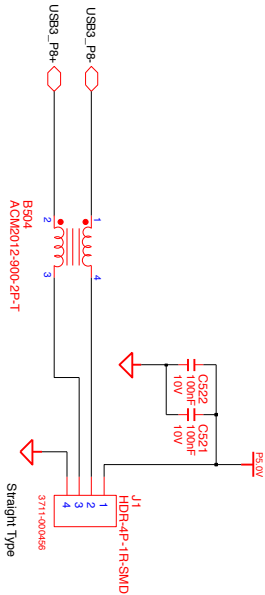
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ROUTE CODE	LSF EDIT	June 09, 2008 11:54:01 AM	PAGE 19	OF 64

TOUCHPAD

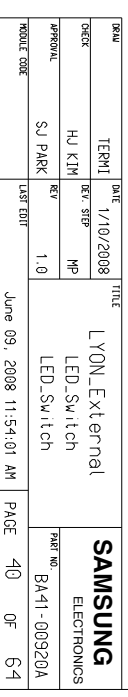


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ROUTE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	62	OF 64

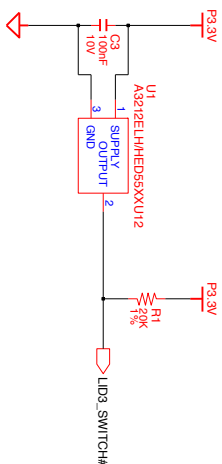
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ROUTE CODE		LAST EDIT	June 09, 2008 11:54:01 AM	PAGE	20	OF 64



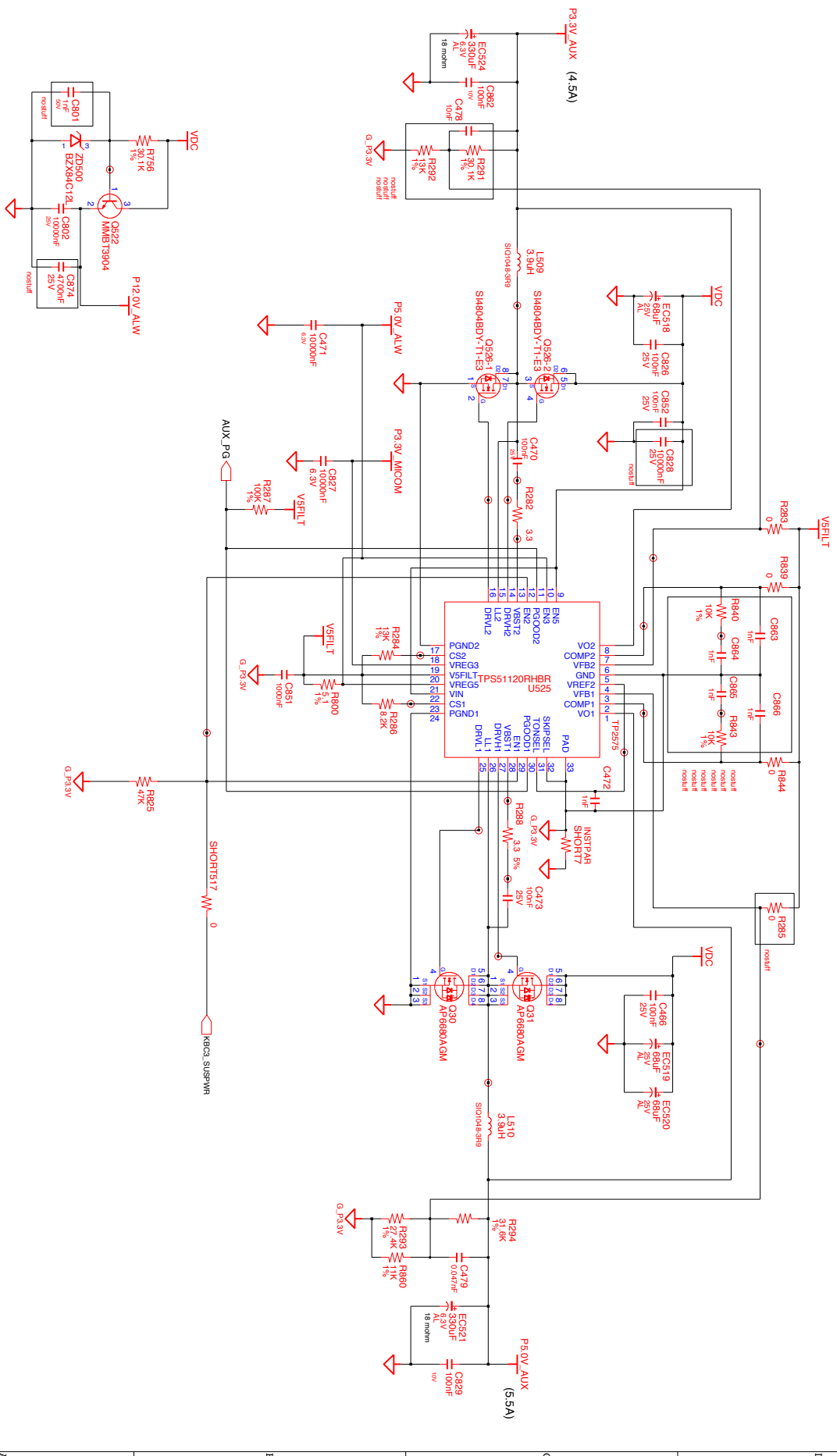
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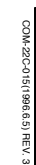
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ROUTE CODE	LSF EDIT	1.0	LID_Switch	BA41-00920A
		June 09, 2008 11:54:01 AM	PAGE	41 OF 64



P3.3V_AUX & P5.0V_AUX



REV	DATE	TITLE	SAMSUNG
001	1/10/2008	LYON-External	
002	REV. STEP	PUR.MV-3V-5V	
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004	REV	P3.3V_AUX / P5.0V_AUX	
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007	REV	PAGE 53 OF 64	
008	REV	BA-41-00920A	
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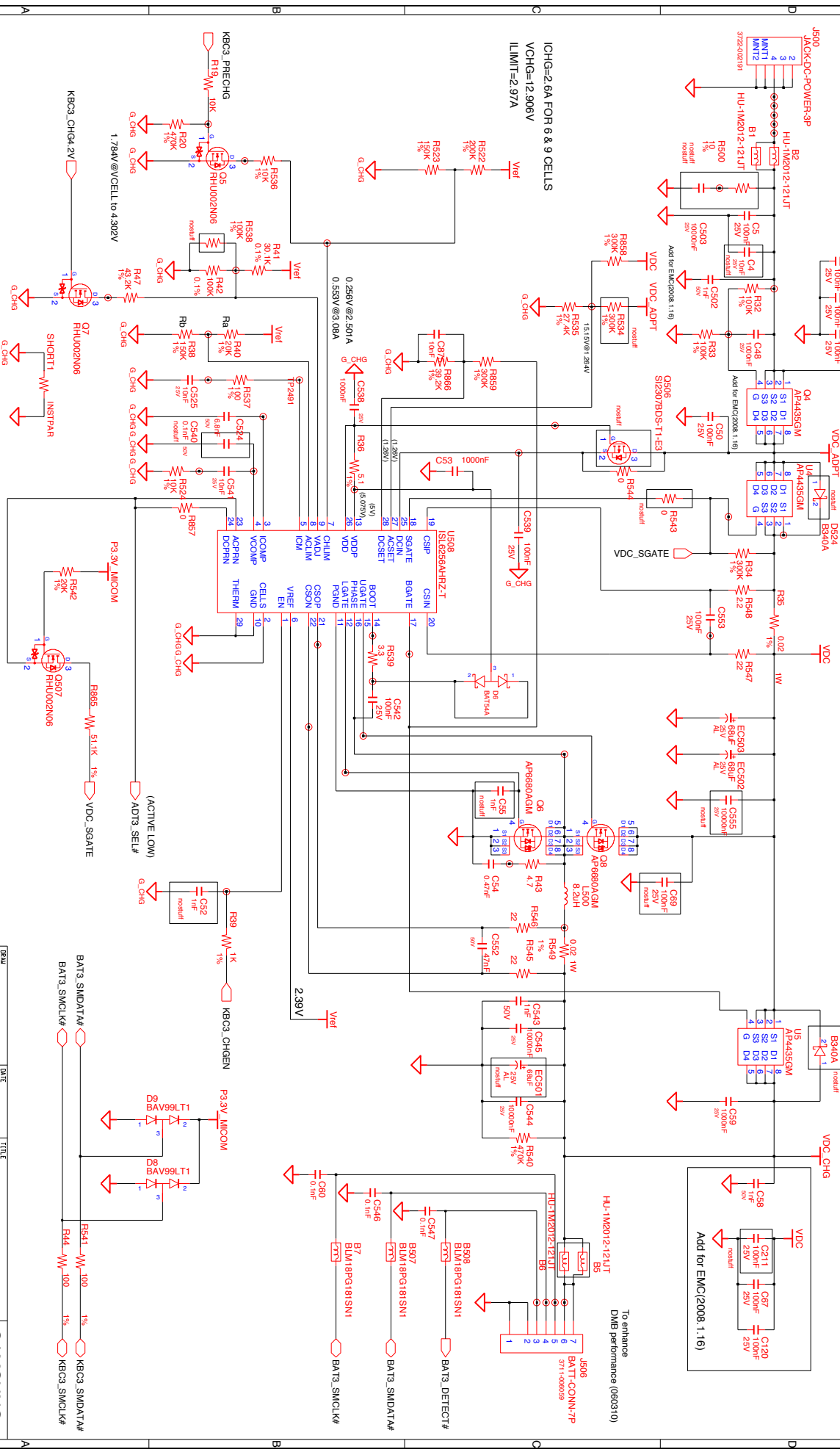


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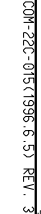
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Add for EMC(2008.1.16)

CHARGER & POWER MANAGEMENT



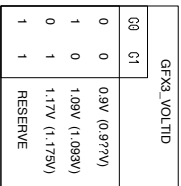
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9.9	2008.11.01	Revise	SJ	MP
10.0	2008.11.01	Revise	SJ	MP

SRP Sheet Number: 71 of 73

The schematic diagram illustrates the power management section of the SC4690MLTBT. It features several voltage regulators and their associated components:

- P1.8V AUX:** A voltage regulator (P1.8V AUX) with a feedback network consisting of resistors R813, R811, and R814. It is connected to the P1.8V AUX pin (pin 11) and the VTTN_1 pin (pin 13).
- VDC:** A voltage regulator (VDC) connected to the VDC pin (pin 12) and the VTTN_2 pin (pin 14).
- P5.0V AUX:** A voltage regulator (P5.0V AUX) with a feedback network consisting of resistors R828, R829, and R830. It is connected to the P5.0V AUX pin (pin 15) and the VTTN_3 pin (pin 16).
- P5.0V:** A voltage regulator (P5.0V) connected to the P5.0V pin (pin 17) and the VTTN_4 pin (pin 18).
- MEM1_VREF:** A voltage reference (MEM1_VREF) connected to the MEM1_VREF pin (pin 19) and the VTTN_5 pin (pin 19).
- Capacitors:** Various capacitors are used for decoupling and filtering, including C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000.
- Resistors:** Various resistors are used for current limiting, feedback, and pull-up/pull-down, including R815, R816, R817, R818, R819, R820, R821, R822, R823, R824, R825, R826, R827, R828, R829, R830, R831, R832, R833, R834, R835, R836, R837, R838, R839, R840, R841, R842, R843, R844, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900.
- Other Components:** The diagram also shows a battery (BAT54A), a diode (D519), and a capacitor (C850).

DATE	TITLE		SAMSUNG	
ORDER	TEPH	LYON_External	ELECTRONICS	
REV.	REV. STEP	PAR_MV_Memory		
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REV	1.0			
TABLE CODE	LIST EDIT	June 09, 2008 11:54:01 AM	PAGE	57 OF 64
undefined				



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CHECK	REV: SGP	MP	PART NO. BA-41-00929A		
APPROVAL	REV	1.0	Bxt Gfx Core (SC471)		
PROJECT CODE	LSI EDIT	June 09, 2008 11:54:01 AM	PAGE	2	OF 2

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Sheet40	-----	Gfx_External_Nvidia_Nb9x_64bit[sheet3]			
Sheet41	-----	Gfx_External_Nvidia_Nb9x_64bit[sheet4]			
Sheet42	-----	Graphics_Memory_Nvidia[sheet1]			
Sheet43	-----	Graphics_Memory_Nvidia[sheet2]			
Sheet44	-----	PCIE_Minicard_Slot[sheet1]			
Sheet45	-----	HDA_Codec_Alc262[sheet1]			
Sheet46	-----	HDA_Codec_Alc262[sheet2]			
Sheet47	-----	HDA_Codec_Alc262[sheet3]			
Sheet48	-----	HDA_Codec_Alc262[sheet4]			
Sheet49	-----	MICOM_Renesas2110_100p[sheet1]			
Sheet50	-----	HDD_IF_Conn[sheet1]			